NEUROMORPHIC ENGINEERING

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Contents

Summary

Neuromorphic engineering is an interdisciplinary field that attempts to map the brain's computational principles onto a physical substrate. Neuromorphic systems often combine brain-inspired computation and processing devices and use biomimetic sensors for data input. The components are implemented as VLSI integrated circuits or systems-on-chip (SoCs), fabricated in state-of-the-art semiconductor fabrication technologies, and are assembled into embedded multi-chip systems to be integrated into a variety of application platforms from humanoid robots to unmanned aerial vehicles (UAVs).

This chapter discusses the most common bio-inspired communication strategies, the principles of computation using neuromorphic Very Large Scale Integration (VLSI) neurons, and peripheral sensory transduction and processing of the kind performed by biological retinas and cochleas.

1. Introduction

Despite all the impressive progress made during the last decades in the fields of information technology, microelectronics and computer science, artificial sensory and information processing systems are still much less effective in dealing with real-world tasks than their biological counterparts. Even small insects outperform the most powerful computers in routine functions involving e.g. real-time sensory data processing, perception tasks and motor control and are, most strikingly, orders of magnitude more energy-efficient in completing these tasks. The reasons for the superior performance of biological systems are only partially understood, but it is apparent that the hardware architecture and the style of computation are fundamentally different from what is state-of-the-art in artificial clocked information processing.

Very generally speaking, biological neural systems rely on a large number of relatively simple, slow and unreliable processing elements and obtain performance and robustness from a massively parallel principle of operation and a high level of redundancy where the failure of single elements usually does not induce any observable system performance degradation. Studying and understanding the computational principles of the brain and how they can be exploited to build intelligent artificial systems are fundamental for devising a new generations of neuromorphic systems, that, as the biological systems they model, are adaptive, fault-tolerant and scalable, and process information using energy-efficient, asynchronous, event-driven methods.

Neuromorphic engineering is an interdisciplinary field that attempts to map the brain's computational principles onto a physical substrate. Carver Mead, who has pioneered the field in the late 1980's, showed that the physics governing the Complementary Metal–Oxide–Semiconductor (CMOS) transistor operating in the sub-threshold regime is analogous to that of the trans-membrane ionic channel (Mead, 1989a). Exploiting such physical similarities between the electrical and the biological fundamental primitives of computation allows constructing electronic circuits that implement e.g. models of voltage-controlled neurons and synapses, or biological computational functions such as photo-transduction, multiplication, inhibition, correlation, thresholding, or winner-take-all selection.

Neuromorphic systems often consist of a hybrid of analog and digital technologies. In this chapter we will focus on neuromorphic devices and systems based on analog neural circuits. These neural circuits perform non-linear analog computation (e.g. a non-linear integration of impinging synaptic currents or external cues) and the generation of digital events representing neural action potentials. In this way, the communication can be realized in an event-based, power-efficient fashion. Because computations are instantiated on analog circuits operating in parallel, these systems can be designed to operate in real-time, thereby enabling them to easily interact with real-world environments. Neuromorphic devices are easily scalable because many of the computations taking place in the neurons can be captured by simple circuits (e.g. the Integrate & Fire (I&F) neuron) which can be densely implemented on the chip, and multiple chips can be combined to form a large multi-chip system using event-based communication. Because these exploit the analog properties of the substrate, they are potentially more power-efficient than general-purpose digital processing technologies.

In this chapter, we will discuss the most common event-based communication strategies, the principles of computation using neuromorphic Very Large Scale Integration (VLSI) neurons, and peripheral sensory transduction and processing of the kind performed by biological retinas and cochleas.

2. Neuromorphic Communication

To build complex neuromorphic systems with significant computational power and high flexibility we need to resort to multi-chip systems. For example, a common strategy is to separate the sensing stage (silicon retinas, silicon cochleas) from further computing stages (spiking neural networks), transmitting signals between chips. In this case, the main advantages are the possibility of achieving higher density in the sensing stage, allowing convergence of the output of multiple sensors to a single processing stage, divergence from one sensor to multiple processing modules, and constructing hierarchical processing stages using multiple instances of the same chip. However, in these systems the connectivity across chip boundaries is severely limited by the small number of input-output connections available with standard chip packaging technology (of the order of a few hundreds pins).

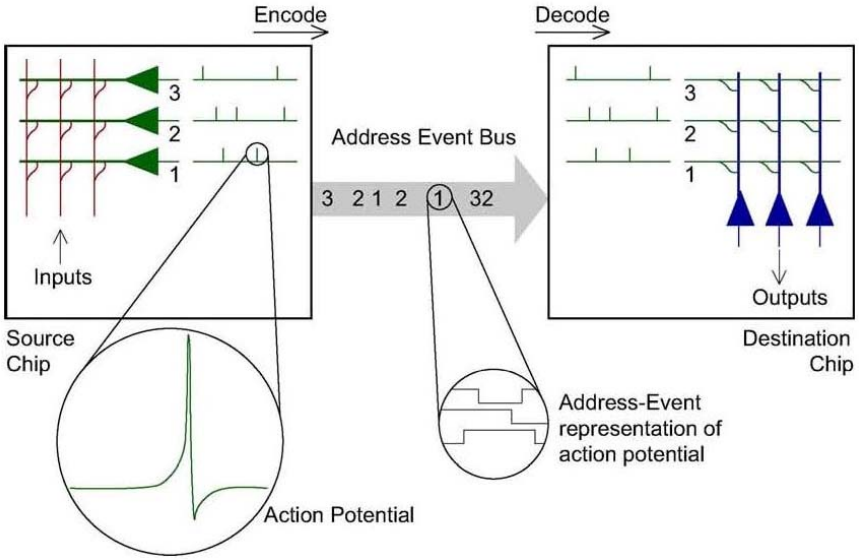

Figure 1. Schematic diagram of an AER chip-to-chip communication example (adapted from (Deiss et al., 1998)). The address event bus transmits the encoded address of a sending node on the source chip as soon as it generates an event. On the receiver chip, the incoming address events are decoded and transmitted to the corresponding receiving node.

One strategy for overcoming this problem is to use time-division multiplexing. The activity of analog VLSI neurons, as for biological neurons, is typically low frequency, from a few Hz to a couple of hundred Hz. The speed of digital buses (gigahertz) can be traded for connectivity among spiking networks by sharing a few wires to communicate (infrequent) events. If the signals to be transmitted across chips are encoded by spikes (i.e. stereotyped non-clocked digital pulses), as it is the case for most neuromorphic devices, an efficient communication protocol that can be used is based on the Address

Event Representation (AER) (Boahen, 1998; Deiss et al, 1998; Lazzaro et al, 1993; Mahowald, 1992a). In this representation, input and output signals are real-time, digital events that carry analog information in their temporal structure (inter-spike intervals).

The AER uses binary-encoded words to represent address events and send them on an asynchronous communication channel. Each word encodes the address of the sending node (see Fig. 1). Events generated by sending nodes are communicated through the channel to one or more external receivers. Different approaches are available for the transfer of the data between the transmitting array of neurons and the channel (e.g. sequential scanning, ALOHA access protocol, priority encoder). A comparative study of access topologies for Address Event (AE) communication channels has been presented in Culurciello and Andreou (2003).

2.1. Arbitrated AER for Multi-chip Systems

Typical topologies and sizes of most recent neuromorphic implementations, with sending nodes in the order of hundreds of thousands, encourage the choice of arbitrated AER as opposed to other access topologies.

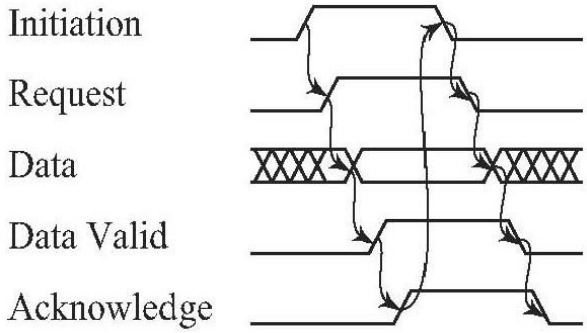

Figure 2. Point-to-Point handshake protocol. A node within the sender chip initiates a handshake cycle by prompting the sender to make a request (initiation signal). After making a request, the sender puts the data on the address event bus. Since the address lines may take different amounts of time to stabilize a data valid line is used to signal when the data on the address bus are set. The receiver acknowledges receipt of the data and the initiation signal is reset to let the sender drop the request and complete the handshake cycle.

The arbitrated AER protocol originally proposed by Mahowald (1992a) is for single sender, single receiver systems. This is known as the Point-to-Point (P2P) AER protocol (AER-Caltech-Memo, 1993). The process of sending events from one chip to the other is regulated by a handshake (see Fig. 2). A simple *handshake* involves two chips:
a *sender chip* and a receiver chip. A node in the sender chip initiates an event by activating a *request signal*. The receiver chip must answer the request by activating an acknowledge signal, after which it reads the data on the address-event bus. After the acknowledge signal is activated, the sender chip removes the request to let the receiver chip remove the acknowledge signal. The handshake cycle is completed when the acknowledge signal is removed by the receiver chip, and another cycle can be initiated by a node in the sender chip.

Systems containing more than two AER chips can be assembled using additional, offchip arbitration. These off-chip arbiters can also use lookup-tables and processing elements to remap, time-stamp and perform digital operations on address-events (Dante et al, 2005; Deiss et al., 1998). The P2P protocol is not suitable for multi-chip systems because the sender drives the address bus, shared by all senders in this case, as a consequence of activating the request. In a multi-chip system only the acknowledged sender should drive the address bus, to prevent data corruption in case two senders attempt to send an event at the same time.

Deiss et al. (1998) proposed the SCX-1 Local Address-Event Bus (LAEB) for multi-chip AER systems (SCX stands for Silicon Cortex, see Section 2.2). The authors presented a communication protocol for multiple senders and multiple receivers on the same address bus. Each chip connected to the local address bus has a dedicated pair of request and acknowledge lines. The handshake protocol is represented in Fig. 3.

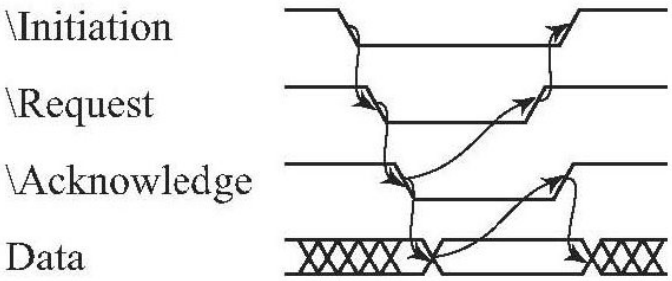

Figure 3. SCX handshake protocol. A node within the sender chip initiates a handshake cycle by prompting the sender to make a request. The sender can write the data on the AE bus only after the receiver acknowledges. The handshake cycle is complete only when both request and acknowledge are reset.

A recent successful evolution of the AER is the burst-mode “word-serial" address-event link proposed by Boahen (2004c, 2004b, 2004a). This design uses address-events to communicate between cells in the same or in different bidimensional arrays. Row and column addresses are not transmitted in parallel, as in previous designs, but serially. The loss in speed due to serial transmission is compensated by not retransmitting the row address if the next event is from the same row: row activity is encoded in a burst consisting of the row address followed by a column address for each active cell. Multi-chip systems can be built in a chain extending the single-transmitter-single-receiver link using mergers and splitters. The merger circuit combines the address events at its input with address events generated by the neuron array and sends them off chip via a transmitter. The splitter circuit makes two copies of the AER events appearing at its input. See (Choi et al, 2005) for an example of such architecture.

2.2. AER Hardware Infrastructures

The hardware infrastructure is an essential instrument to fully characterize neuromorphic prototype chips. This infrastructure has to provide ways to stimulate and monitor the activity of a single chip. In addition, it has to be able to interface several chips and dynamically define the connectivity among them, implementing complex

multi-chip systems. Furthermore, it should allow logging of data from all chips, allowing off-line analysis.

Different approaches can be pursued to build neuromorphic multi-chip systems: dedicated full-custom circuits can be implemented to support specific AER devices, or a general-purpose full-custom architecture can be designed to host any AER device compliant to a certain standard. Several multi-chip systems have been implemented with both approaches. Examples of dedicated full-custom multi-chip systems are described in Choi et al. (2005) and Higgins & Koch (2000). These systems comprise EPROMs or FPGAs for remapping of the addresses, but they do not include any device to store the activity of the AER chips (requiring a separate acquisition instrument, usually a logic analyzer, to look at the system behavior) or to stimulate the chips with synthetic trains of spikes.

In the late 1990's and early 2000's several research groups (e.g. (Deiss et al., 1998; Serrano-Gotarredona et al., 2005; Chicca et al., 2007)) devoted considerable efforts to the development of general architectures to interconnect, monitor and stimulate several AER devices. The first example of a general-purpose multi-sender multi-receiver communication framework for AER devices, called Silicon CorteX (SCX), is the one proposed by Deiss et al. (1998). SCX is a fully-arbitrated AE infrastructure which can support up to six AER chips; larger systems can be assembled by linking together multiple boards. SCX provides a method of building a distributed network of local busses sufficient to build an indefinitely large system, coordinating the activity of multiple sender/receiver chips on a common bus. The user can configure arbitrary connections between neurons, set analog parameters and monitor the activity of the neurons.

In the context of the CAVIAR project (CAVIAR is the acronym of the European funded project IST–2001–34124: Convolution AER Vision Architecture for Real Time), Serrano- Gotarredona et al. (2005) proposed a distributed system in which a USB-AER board can be programmed to perform one of five different functions: (1) mapping of addresses, (2) capture of timestamped AEs, (3) reproduction of time-stamped sequences of AEs in real time, (4) transformation of sequence of frames into AEs in real time, (5) histogram AEs into sequences of frames in real time. Additional PCBs are used to record AE traffic on the AER bus; split one AER bus into 2, 3 or 4 buses; merge 2, 3 or 4 AER busses into a single bus; and capture time-stamped AEs to a computer.

The hardware infrastructure described by Chicca et al. (2007) consisted of a single full custom general purpose PCI board (the PCI-AER board) hosted in a workstation, that allowed connection of up to four sender and four receiver chips, arbitrary intra- and interchip connectivity, stimulation of receiver chips with synthetic trains of spikes, monitoring and logging for the activity of all sender devices. Because of the requirement of a host workstation this system was not as portable as the CAVIAR system, nevertheless it proved to be very convenient for rapid prototyping tests and online reconfigurability.

An alternative but comparable infrastructure composed of an AER mapper and a dedicated serial AER interface with flow control was proposed more recently (Fasnacht

et al, 2008; Fasnacht & Indiveri, 2011). This system provided improved figures in terms of achievable event rates and minimization of event latencies.

Large-scale AER communication architectures (e.g. the SCX) allow to prototype multineuron experiments, and to combine with other neuromorphic devices such as neuromorphic sensors. Given the rapidly increasing size of the emulated neural networks, nowadays AER infrastructures are often faced with scalability problems, which are being addressed with different strategies by several research groups.

At Stanford University, Kwabena Boahen's and colleagues developed programmable analog neurocore chips which emulate over 65'000 neurons each and are assembled on a 16 chips array containing over a million neurons (Neurogrid project, (Silver, Boahen, Grillner, Kopell, & Olsen, 2007)). An AER packet network is used to communicate spikes between chips. A binary tree organization of the chips grid is supported by local routers with dedicated RAMs for storing connectivity information. The connectivity pattern in the Neurogrid is optimal for implementing cortical columns.

Gert Cauwenberghs and colleagues (University of California at San Diego) have designed a neuromorphic chip named Integrate and Fire Array Transceiver (IFAT) and the related routing architecture Hierarchical AER IFAT (HiAER-IFAT). A 250'000 neurons system has been demonstrated with this hardware (Park et al, 2012). They extended the AER protocol to a fractal hierarchical architecture, with repeated address buses and communication relays at varying spatial scales.

The European FACETS/BrainScaleS project (FACETS, 2005–2009) targets wafer-scale implementations of spiking neural networks. The spiking neurons are designed to operate about 1000 to 10000 times faster than biological neurons Schemmel et al. (2008), so they can potentially provide a more power-efficient alternative to software simulations of spiking neural networks performed on digital supercomputers. The communication infrastructure for the waferscale neuromorphic system developed within this project (Scholze et al., 2011) consists of a source-synchronous high-speed serial packet communication of timestamped spike events. Packed-based transmission was chosen to deal with the challenging requirement of large number of sources and targets typical of a waferscale system.

3. Sensing

Representing a new paradigm for the processing of sensor signals, neuromorphic systems have succeeded in the emulation of sensory signal acquisition and transduction. Neuromorphic and bio-inspired sensors, like their biological models, implement event-driven processing and feature extraction directly at the sensory device level, massively reducing data redundancy and consequently the demands on transmission power, bandwidth, memory and post-processing power. The visual and auditory senses have been tackled early by the neuromorphic community, yielding a variety of bio-inspired vision sensors (silicon retinas) and auditory sensors (silicon cochleas). Recently, also event-based olfactory and haptic sensory devices are being developed. Neuromorphic electronic devices are usually implemented as VLSI integrated circuits or systems-on-chip (SoCs) on planar silicon, the mainstream technology used for fabricating the

ubiquitous microchips that can be found in practically every modern electronically operated device (Fig. 4).

One of the first working neuromorphic electronic devices was modeled after a part of the human neural system that has been subject to extensive studies since decades – the retina. The construction of an artificial silicon retina has been a primary target of the neuromorphic community from the very beginning. Mahowald and Mead reproduced the first three of the retina's five layers on silicon in 1989 (Mahowald, 1992b). Zaghloul and Boahen implemented simplified models of all five layers of the retina on a silicon chip starting in 2001 (Zaghloul & Boahen, 2004a, 2004b). These chips generate, in real time, outputs that correspond directly to signals observed in the corresponding levels of biological retinas.

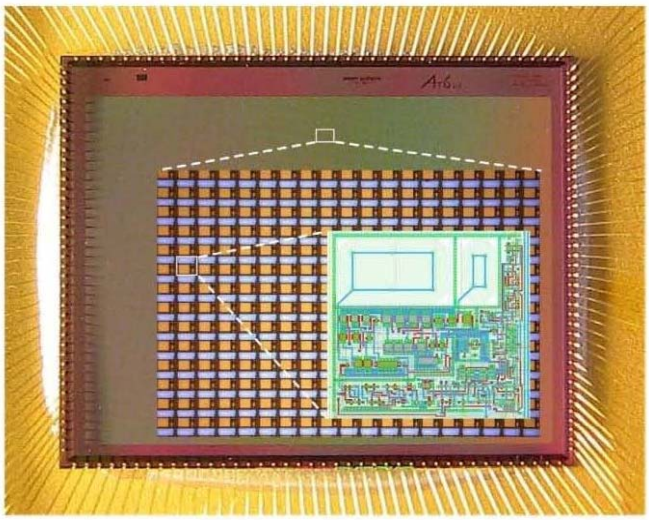

Figure 4. Microscope photograph of a "silicon retina" sensor, part of the pixel array at higher magnification, and the CMOS layout of one pixel cell (Posch et al., 2011).

3.1. AER Vision Sensors - Silicon Retinas

The first silicon retina of Mahowald and Mead models the outer-plexiform layer (OPL) of the vertebrate retina and contains artificial cones, horizontal cells and bipolar cells. A resistive network computes a spatiotemporal average that is used as a reference point for the system. By feedback to the photoreceptors, the network signal balances the photocurrent over several orders of magnitude. The silicon retina's response to spatial and temporal changing images captures much of the complex behavior observed in the OPL. Like its biological counterpart, the silicon retina reduces the bandwidth needed to communicate reliable information by subtracting average intensity levels from the image and reporting only spatial and temporal changes (Mahowald, 1992b; Mead, 1989a; Mahowald, 1994).

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Biographical Sketches

Emre Neftci studied physics from the Federal Institute of Technology Lausanne (EPFL) where he graduated in 2006. He received his Ph.D. degree from the Physics Department of the Federal Institute of Technology Zurich (ETHZ), Switzerland, and a PhD in Neuroscience from the Neuroscience Center Zurich (ZNZ) in 2010. He continued his research as a PostDoc at the Institute of Neuroinformatics at the University of Zurich and ETH Zurich from January 2011 to June 2012. Since August 2012, he is a postdoctoral research fellow in the institute for neural computation at the University of California, San Diego (UCSD). His current scientific interests are the interface between computational neuroscience, machine learning and neuromorphic hardware.

Christoph Posch received the M.Sc. and Ph.D. degrees in electrical engineering and experimental physics from Vienna University of Technology, Vienna, Austria, in 1995 and 1999, respectively. From 1996 to 1999, he worked on analog CMOS and BiCMOS IC design for particle detector readout and control at CERN, the European Laboratory for Particle Physics in Geneva, Switzerland. From 1999 onwards he was with Boston University, Boston, MA, engaging in applied research and analog/mixed-signal integrated circuit design for high-energy physics instrumentation. In 2004 he joined the newly founded Neuroinformatics and Smart Sensors Group at AIT Austrian Institute of Technology (formerly Austrian Research Centers ARC) in Vienna, Austria, where he was promoted to Principal Scientist in 2007. Since 2012, he is co-directing the Neuromorphic Vision and Natural Computation group at the Institut de la Vision in Paris, France, and has been appointed Associate Research Professor at Universite Pierre et Marie Curie, Paris 6. His current research interests include neuromorphic analog VLSI, CMOS image and vision sensors, and biology-inspired signal processing. Dr. Posch has been recipient and co-recipient of several scientific awards including the Jan van Vessem Award for Outstanding European Paper at the IEEE International Solid-State Circuits Conference (ISSCC) in 2006, the Best Paper Award at ICECS 2007, and Best Live Demonstration Awards at ISCAS 2010 and BioCAS 2011. He is senior member of the IEEE and member of the Sensory Systems and the Neural Systems and Applications Technical Committees of the IEEE Circuits and Systems Society. Christoph Posch has authored more than 80 scientific publications and holds several patents in the area of artificial vision and image sensing.

Elisabetta Chicca studied physics at the University of Rome 1 'La Sapienza', Italy, where she graduated in 1999. In 2006 she received a PhD in Natural Sciences from the Physics department of the Federal Institute of Technology Zurich (ETHZ), Switzerland, and a PhD in Neuroscience from the Neuroscience Center Zurich (ZNZ). Immediately after the PhD, she started a PostDoc at the Institute of Neuroinformatics at the University of Zurich and ETH Zurich, where she continued working as Research Group Leader from May 2010 to August 2011. Since August 2011, she is an assistant professor at Bielefeld University and is heading the Neuromorphic Behaving Systems Group based in the Faculty of Technology and the Center of Excellence Cognitive Interaction Technology (CITEC). Elisabetta Chicca is member of the IEEE NSA and BioCAS technical committees, Secretary of the IEEE NSA technical committee, and associate editor of Frontiers in Neuromorphic Engineering.