SMART POWER INTEGRATED CIRCUITS

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Contents

Summary

Integrated circuits can be analog, digital or power circuits. According to the requirements there exist different technologies: bipolar, MOS or power technologies. *Smart power* technologies offer the integration of analog and digital circuits combined with the power stages on the same chip. The *smart* part of the smart power circuits adds diagnostic and protection functions to the power transistors. This increases the robustness and reliability of power drivers for automotive and industrial applications. The application range goes from protected low side, high side and bridge driver configurations to complete smart power system ICs.

1. Introduction

Today power technologies make it possible to add on chip diagnostic functions and protection circuits for electronic power switches. This combination of power devices and analog and digital circuits is called “Smart Power” circuits. It is a kind of

monolithic system integration, including the power devices. There are many automotive and industrial applications which can use these smart power integrated circuits. As an example for automotive applications there exist intelligent power switches for controlling the ABS-braking system, system power chips for airbag control, for engine management of the car, switched mode supplies, intelligent switching of all lights and so on. Additional to normal functionality the smart power circuits has to withstand some hostile environment conditions like high voltages, high temperatures, short circuit and overvoltage conditions and they have to fulfill high reliability requirements.

2. Smart Power Technologies

Smart Power technologies make it possible to combine logic, analog functions and multiple power output stages on one chip. There is no single power technology which could be chosen as the best for all applications. Classification of smart power technologies is based either on the isolation technique or on the type of the power device, including the path of current flow. Common to all smart power technologies is the combination of a DMOS-type power transistor with standard CMOS and/or bipolar components for the analog and control functions.

2.1. Self Isolation

"Self isolation" is the simplest solution and it is used in any MOS process (Figure 1). Isolation of neighboring components is only done by applying the right voltages to the components in respect to the substrate or well connection. In an n-substrate (or inside of an n-well) there two or more p-channel MOS-devices can be arranged without need of additional isolation-means. To obtain isolation the p-n junctions from the active device to the substrate (drawn as diodes in Figure 1) has to maintain in *off*-condition. Therefore the voltage applied to the substrate ($+V_{dd}$) has to be higher as the voltage which is applied to the p-channel devices. In a similar way n-channel MOS transistors can be arranged inside a p-well which has to be connected to a negative voltage to obtain self isolation.

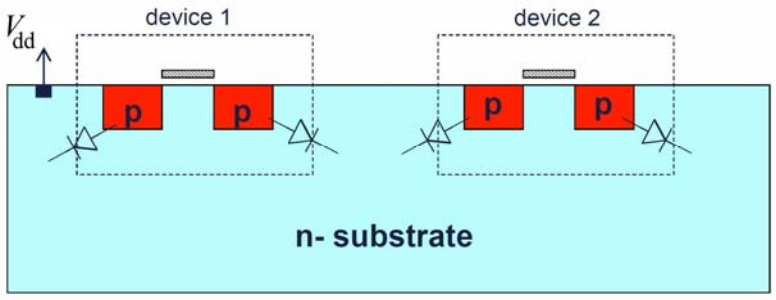

Figure 1. Self isolation approach

The first step to facilitate a technology for smart power applications is to expand the voltage capability of the MOS transistors. This can be done by inserting a lightly doped drain extension in series to the channel. For a p-channel MOS this drain extension is a high ohmic, low doped p- diffusion, for an n-channel MOS an n- diffusion is used, see Figure 2.

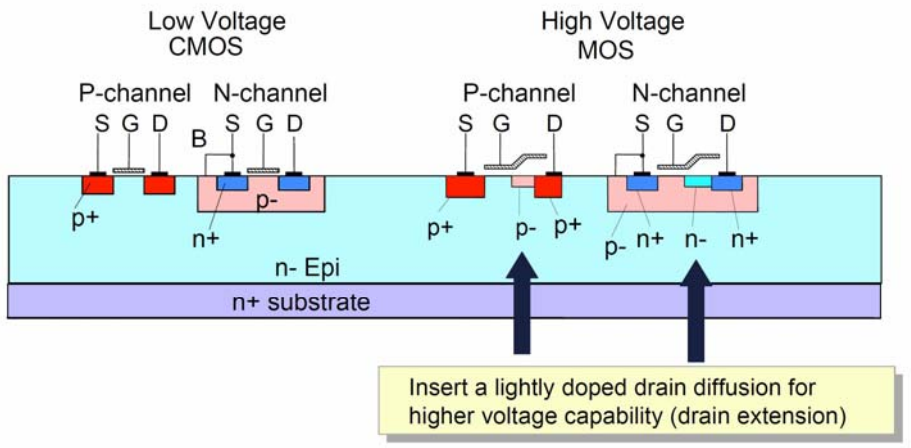

Figure 2. Expand the voltage capability of MOS transistors

This drain extension increases the voltage capability drain to source to the required value, e.g. 60 V for automotive applications or also more, if needed. The voltage capability can be adjusted by the length and the doping concentration of the drain extension. To avoid break-trough of the thin gate oxide the poly-gate needs higher distance (thicker oxide) over the drain extension area.

The next step is to introduce a high voltage power transistor. In a self isolation process with n-substrate the most efficient way is the vertical n-channel DMOS-transistor (Figure 3).

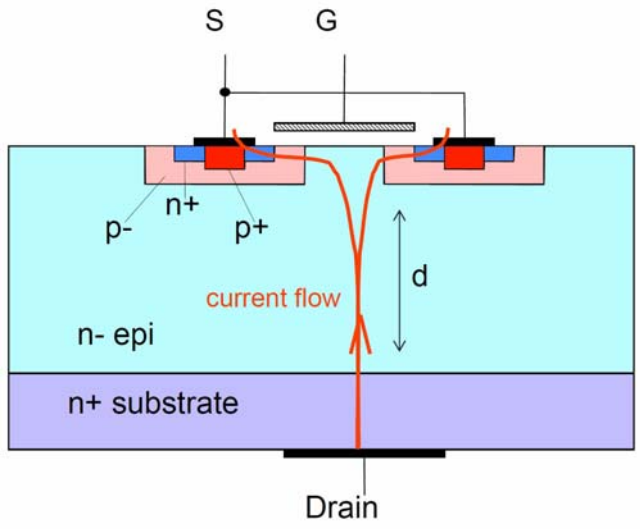

Figure 3. Vertical DMOS power transistor

This transistor consists of a channel, which is controlled by a gate voltage like a low voltage MOS transistor. But the drain is then connected to the backside of the chip, directly to the n+ substrate and the n- epi layer is used as drain extension. Voltage capability is designed by choosing thickness (d) and doping of the epi layer, as a thumb rule you can calculate with 10V for any µm of epi thickness. Therefore e.g. smart power

processes with 60V capability are in the range of $d = 6\mu$ epi layer thickness. To avoid additional voltage drop in the vertical drain path the wafer material itself (substrate) is high doped to allow a low ohmic drain connection. The backside of the chip needs also a metallization (usual aluminum) for a good contact to the package. For high current capability many DMOS cells are switched in parallel, these results in power transistors with a very low Rds(on) and a reasonable chip area.

The described power transistor has a *lateral* channel (close to the surface) and a *vertica*l drain extension. To save further chip area also the channel could be realized in a vertical way. This is possible using trench etching technology. This *trench* power transistor is the best device in respect to Rds(on) and chip area ratio (see Figure 4). Trench MOS transistors exist as discrete devices and are also used in advanced smart power technologies.

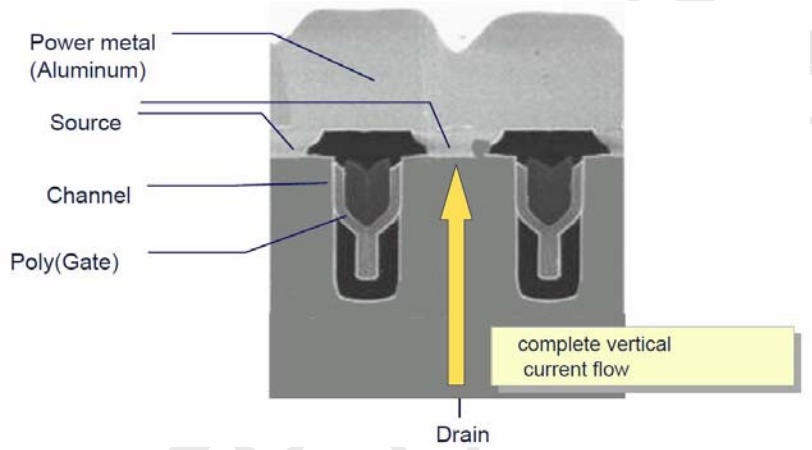

Figure 4. Trench DMOS power transistor

The combination of low voltage CMOS, high voltage MOS and vertical DMOS power transistors on one chip results in a self isolation smart power process, shown in Figure 5.

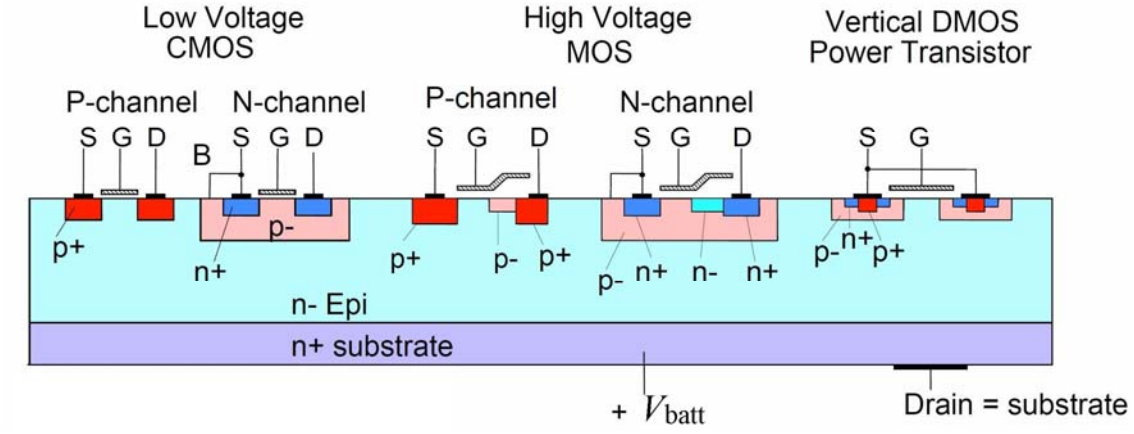

Figure 5. Cross section of a self isolation smart power technology

The substrate is the drain of the power transistor, it has to be connected to the positive supply voltage (according self isolation) and therefore the drain of the DMOS is fixed to the positive supply line (see Figure 6). This makes this technology very well suited for low-resistive, high current high side switches with common drain.

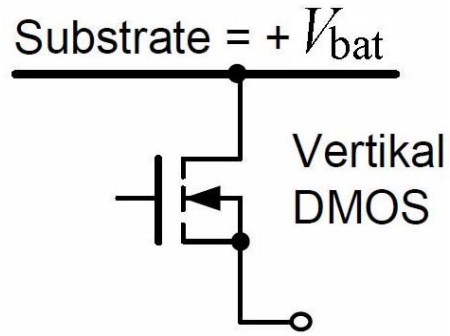

Figure 6. Drain of DMOS is fixed to substrate (positive supply voltage)

2.2. Junction Isolation

Junction isolation is mainly known from bipolar technologies. If it is used for Smart Power technologies, the advantage is that also bipolar devices can be realized in addition to MOS and high voltage MOS devices. This gives a higher flexibility for analog circuit design.
Based on a p-substrate and an n-doped epitaxial layer the separation of the devices is obtained through reverse-biased junctions realized by diffused p-regions (p-iso), as shown in Figure 7.

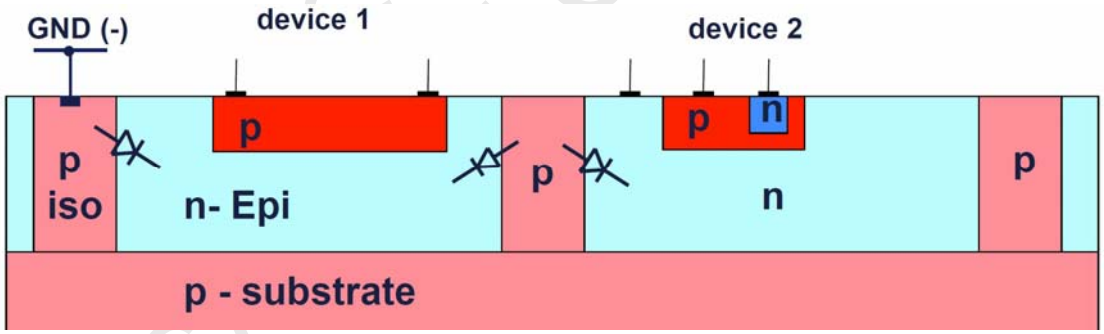

Figure 7. Junction isolation

To obtain the isolation the substrate has to be connected to the most negative voltage (e.g. GND) in respect to the voltages applied to the n-epi wells.

An example of a junction isolated smart power technology is shown in Figure 8. The junction isolated n-wells can be used to integrate CMOS logic circuits, bipolar transistors and also vertical DMOS power transistors. The drain connection of the DMOS is brought to the surface via a buried layer and sinker, also called an up drain configuration. This approach allows the integration of one or more isolated DMOS power devices connected in any configuration. It gives more flexibility in the

application of power transistors as compared to the self isolation approach; low side, high side and bridge configurations are possible. This combination of bipolar, CMOS and DMOS devices on one silicon is also called *BCD* process and can be used to design a high variety of smart power integrated circuits.

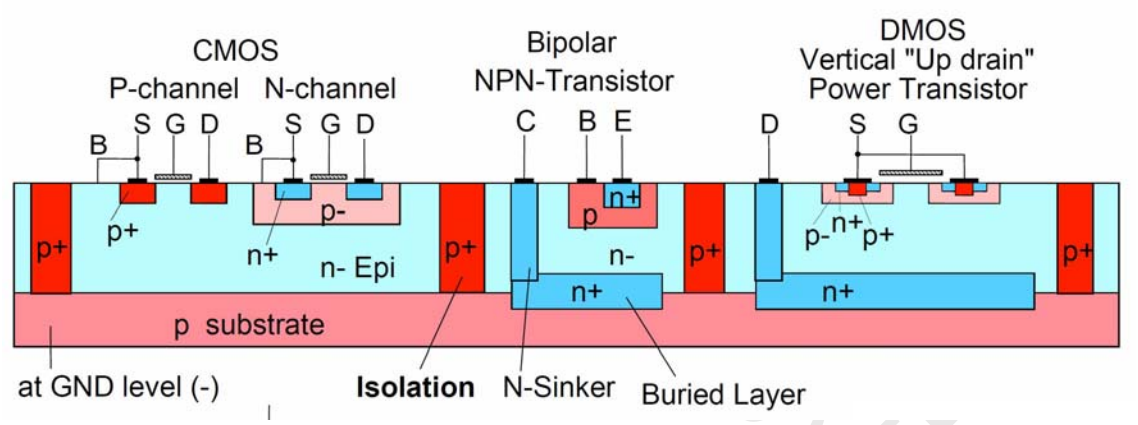

Figure 8. Cross section of a junction isolated smart power technology (BCD)

The low voltage p-channel and n-channel transistors allow us to integrate CMOS logic parts into the power switches. The bipolar transistors are provided for the analog circuits due to the better characteristics like noise, offset and drift behavior.

2.3. Dielectric Isolation

Dielectric isolation (DI) provides a separation between different devices on a chip not only with p-n junctions but with real insulators using silicon oxide (Figure 9). The advantage of this concept are less bulk parasitic effects against substrate and between the devices; lower leakage currents and smaller chip area for high voltage components. But there are also disadvantages: the thermal conductivity of oxide is very low compared to that of silicon; this increases the thermal resistance and limits the possible integration of power device. To insert a buried oxide layer inside a chip below the active devices requires a more complex and costly manufacturing process. Due to this DI is an expensive technology and therefore not the mainstream for smart power circuits.

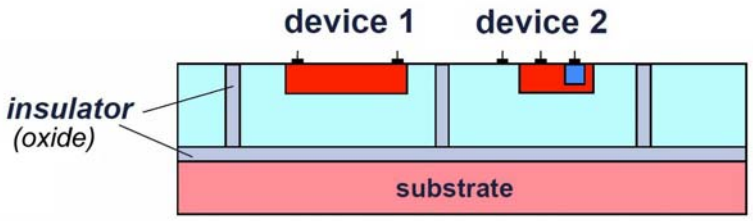

Figure 9. Dielectric isolation, Silicon on Insulator (SOI)

A variant of the dielectric isolation is the *Deep Trench Isolation* (DTI) which uses oxide to separate the components in lateral direction but not against the substrate, see Figure 10. The advantage here is no limitation in heat transfer for power devices and a chip

area reduction for high voltage components, because the oxide filled trenches are significant smaller then the p-so diffusion areas used in a junction isolation process. But bulk parasitic problems and leakage currents against substrate are similar as in junction isolation technologies.

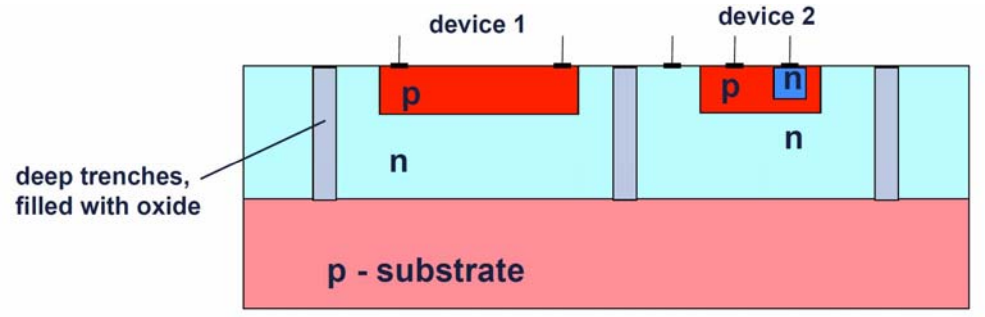

Figure 10. Partial dielectric isolation, Deep Trench Isolation (DTI)

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Biographical Sketch

Heinz Zitta received the M.Sc. degree in Electrical Engineering from the Technical University of Vienna in 1977. From 1977 to 1984 he was with Philips, Vienna, as a designer for audio and video products. In 1984 he joined Siemens (now Infineon) Design Center for Microelectronics in Villach, Austria as a designer for bipolar and high-voltage CMOS products. Next step was the design of many smart power products for automotive applications like ABS- and airbag systems and engine management applications. He holds several patents in circuit design and published some conference papers in the field of smart power topics. Academic appointments include teaching at the Carinthia University of Applied Sciences and at the Technical University of Graz, Austria.