# INSULATION CO-ORDINATION IN POWER SYSTEMS

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#### Contents

- 1. Introduction
- 2. Overvoltages in Power Systems
- 2.1. Classification of overvoltages
- 2.2. Temporary overvoltages
- 2.3. Slow-front overvoltages
- 2.4. Fast-front overvoltages
- 2.5. Very fast-front overvoltages
- 3. Surge Arresters
- 3.1. Introduction
- 3.2. Valve type arresters
- 3.2.1. Gapped silicon carbide arresters
- 3.2.2. Gapless metal oxide arresters
- 3.2.3. Gapped metal oxide arresters
- 3.3. Characterization of metal oxide surge arresters
- 3.3.1. Arrester characterization
- 3.3.2. Protective characteristics
- 3.3.3. Energy capabilities
- 3.3.4. Metal oxide surge arrester characteristics
- 3.4. Metal oxide surge arresters models
- 3.5. Selection of metal oxide surge arresters
- 3.5.1. Introduction
- 3.5.2. Protective levels
- 3.5.3. Procedure for arrester selection
- 3.5.4. Phase-to-phase transformer protection
- 3.5.5. Arrester selection for distribution systems
- 3.6. Surge arrester protection
- 4. Insulation Characterization
- 4.1. Introduction
- 4.1.1. Definitions
- 4.1.2. Standard waveshapes
- 4.1.3. Insulation levels
- 4.1.4. Statistical insulation levels
- 4.2. Dielectric strength for switching surges

- 4.2.1. Phase-to-earth strength
- 4.2.2. Phase-to-phase strength
- 4.3. Dielectric strength under lightning overvoltages
- 4.3.1. Standard lightning impulses
- 4.3.2. Nonstandard lightning impulses
- 4.4. Dielectric strength for power-frequency voltage
- 4.5. Atmospheric effects
- 5. Insulation Co-ordination
- 5.1. Introduction
- 5.1.1. Objectives
- 5.1.2. Insulation level
- 5.1.3. Insulation co-ordination approaches
- 5.2. Insulation co-ordination procedure
- 5.2.1. Determination of the representative voltages and overvoltages
- 5.2.2. Determination of the co-ordination withstand voltages
- 5.2.3. Determination of the required withstand voltages
- 5.2.4 Selection of the standard rated insulation level
- 5.3. Case studies
- 5.3.1. Case study 1
- 5.3.2. Case study 2
- 6. Conclusion
- Glossary
- Bibliography
- **Biographical Sketches**

#### Summary

Voltage stresses in power systems can have internal or external origin. Overvoltages can be caused by faults, switching operations or lightning strokes. In addition, they can occur with very wide range of waveshapes and durations. Dielectric failures in power systems can cause tripping of the protective devices, destruction of equipment, or interruption of operation. The breakdown characteristics of the different types of insulation depend on the configuration and environment of the insulation, as well as on the waveshape and duration of the applied voltage. On the other hand, both stresses and withstand insulation voltages may exhibit a random behavior. Therefore, it is important not only to assess the overvoltages that can appear on a given component but the behavior of its insulation taking into account that stress and withstand characteristics may be random.

The goal of insulation co-ordination is to select the electric strength of equipment in relation to the voltages which can appear on the system where the equipment has been or will be installed, and taking into account the service environment as well as the characteristics of the available protective devices. An insulation co-ordination procedure relates the insulation characteristics (strength) to the overvoltages on the system (stress), and accounts not only for risks of failure but for economic and environmental factors. An insulation co-ordination procedure is aimed at determining the lowest values of the insulation withstand voltages in order to meet a performance criterion when equipment is subjected to the representative overvoltages under service conditions. Procedures for

insulation co-ordination have been presented in standards, namely IEC and IEEE. This document is mostly based on the procedure proposed by IEC.

The chapter presents: (i) a short summary of the main types of overvoltages, their causes and the factors that affect their magnitude and shape; (ii) an introduction to metal oxide surge arresters, their protective characteristics and their selection; (iii) a characterization of insulation; (iv) a description of the insulation co-ordination procedure proposed by IEC. The document includes two case studies aimed at illustrating methods for obtaining representative overvoltages, analyzing insulation behavior, and selecting standard insulation levels.

## 1. Introduction

Increase in electrical energy demand has promoted an increase in the voltage of transmission systems; as an example, AC and DC transmission lines above 500 kV are now in operation. The cost of equipment is closely related to the insulation levels that have to be adopted. The choice of insulation level should take into account both the severity of voltage stresses that the system may be subjected to and the probability of occurrence of these stresses.

Power systems are always subjected to overvoltages, which are usually the result of faults, sudden changes in operating conditions caused by switching operations, or the impact of lightning strokes. Therefore, overvoltages can have external origin (e.g., when they are caused by lightning discharges) or internal origin (e.g., when they are caused by switching operations) (Hileman, 1999; Chowdhuri, 1996; Fulchiron, 1995).

In addition, overvoltages can occur with very wide range of waveshapes and durations. The magnitude of external lightning overvoltages remains essentially independent of the system design, whereas that of internal switching overvoltages increases with the operating voltage of the system. As a consequence, with increasing operating voltage a point is reached when the switching overvoltages become the dominant factor in selecting equipment insulation (Hileman, 1999). Up to approximately 300 kV, the insulation has to be designed to withstand primarily lightning surges. For transmission systems above 300 kV the switching overvoltages increase in importance so that at about 550 kV they are equivalent to that of lightning overvoltages. For the highest voltages, 765 kV and above, switching overvoltages in combination with insulator contamination become the predominating factor in the insulation design. Temporary overvoltages are also important since they affect the rating of protective arresters or coordinating gaps which provide a means of controlling the overvoltages.

The different types of insulation – gaseous, liquid and solid – have different breakdown characteristics, which are dependent on the configuration and environment of the insulation, and on the waveshape and duration of the applied voltage. Air still provides the major insulation for transmission networks. An important property of air insulation is that for a given waveshape of the applied voltage the actual breakdown value will vary randomly about a mean value. This characteristic can be represented by the probability of breakdown occurring with a crest voltage, P(V). When computing overvoltages, it is usually assumed that for a large number of switching operations with

different instants of pole closing a normal (Gaussian) switching overvoltage distribution f(V) is obtained. From the two probability distributions, P(V) and f(V), statistical methods are used to determine the risk of failure and to select the specify insulation withstand voltage (IEC 60071-2, 1996).

The purpose of insulation co-ordination is to ensure that the probability of insulation breakdown is limited to an acceptable value and that any breakdown is restricted to selfrestoring insulation. Insulation co-ordination is based on computing the most severe overvoltages occurring on the network and relating them to the breakdown characteristics of the insulation through appropriate margins to obtain withstand voltages for the network components together with the statistical risk of insulation failure.

Procedures for insulation co-ordination are recommended in standards, namely IEC (IEC 60071-1, 2010; IEC 60071-2, 1996) and IEEE standards (IEEE Std C62.82.1; 2010; IEEE Std 1313.2, 1999). The procedure presented in this chapter is that developed by IEC.

IEC Standard 60071 provides a comprehensive guide to coordinating procedures and specifies co-ordination factors and standard insulation levels. According to the IEC, insulation co-ordination comprises the selection of the electric strength of equipment and its application, in relation to the voltages that can appear on the system for which the equipment is intended and taking into account the characteristics of available protective devices, so as to reduce to an economically and operationally acceptable level the probability that the resulting voltage stresses imposed on the equipment will cause damage to equipment insulation or effect continuity of service.

An insulation co-ordination procedure relates the insulation characteristics (strength) to the overvoltages on the system (stress). Although co-ordination is based primarily on determining risks of failure from overvoltage and insulation characteristics, other factors, namely economic and environmental, are involved. The economic factor is always important and includes cost comparisons between overvoltage protection, insulation levels, risk of failure and network outages. Atmospheric factors are also important and their consideration can result in the design of compact lines having both reduced visual impact and transmission corridor width.

The insulation co-ordination procedure takes an iterative approach where several scenarios may be under consideration. From the network configuration and component data, an appropriate simulation of the network is performed to compute representative overvoltages, taking into account the effect of control and protective devices. The breakdown voltage characteristics are based on the type and configuration of the insulation. The procedure relates these two aspects to determine withstand voltages and quantify the risk of insulation failure.

A short summary of the main types of overvoltages, their causes and the factors that affect their magnitude and shape, is presented in Section 2. Surge arresters are one of the main means for limiting overvoltages in power systems, being the gapless metal oxide (MO) surge arrester the most common type presently in use; Section 3 is

dedicated to present the main characteristics of MO surge arresters and how they can be selected. The characterization of power equipment insulation, with emphasis on air insulation, is analyzed in Section 4. Finally, Section 5 details the main principles of the insulation co-ordination procedure developed by IEC.

## 2. Overvoltages in Power Systems

#### 2.1. Classification of Overvoltages

An overvoltage is a voltage, between one phase and earth or between two phases, having a crest value exceeding the corresponding crest of the maximum system voltage.

A first classification of the different types of overvoltage that are likely to occur on power systems considers their origin, and distinguishes two main categories: (i) external and (ii) internal overvoltages.

Standards classify the different types of overvoltages, according to classes and shapes, into four groups (IEC 60071-1, 2010; IEC 60071-2, 1996; IEEE Std C62.82.1, 2010; IEEE Std 1313.2, 1999):

- 1) *Temporary overvoltages*: They are undamped or weakly damped oscillatory phaseto-earth or phase-to-phase overvoltages of relatively long duration (seconds, even minutes). Temporary overvoltages are originated by faults, load rejection, resonance and ferro-resonance conditions, or by a combination of these factors.
- 2) *Slow-front overvoltages*: They are unidirectional or oscillatory overvoltages, with a slow front, highly damped, short-duration. These overvoltages are caused by switching operations, fault initiation, or remote lightning strokes.
- 3) *Fast-front overvoltages*: They are transient overvoltages whose fast front shape is caused primarily by lightning strokes, although they can also be caused by some switching operations or fault initiation.
- 4) *Very fast-front overvoltages*: In general, they are the result of switching operations or faults. These overvoltages are usually associated with high voltage disconnect switch operation in GIS, and with cable connected motors.

Standards also include continuous power-frequency voltages, which are originated with the system under normal operating conditions during which the power-frequency voltage can be expected to vary somewhat but, for the purpose of insulation coordination, is considered to be constant and equal to the highest system voltage for the equipment.

Limitation of overvoltage surges is possible by protective devices. Surge arresters are widely used in electrical power systems, and the superior modern metal oxide surge arresters have renewed interest and widespread use of surge arresters in protection practice. For economic design of equipment and safe operation of power systems, a detailed knowledge of types and sources of overvoltages on power systems is required. A short description of the main causes and methods for limitation of overvoltages is presented is the following subsections.

## **2.2. Temporary Overvoltages**

A temporary overvoltage (TOV) is an oscillatory phase-to-earth or phase-to-phase overvoltage of relatively long duration at a given location which is undamped or weakly damped. In relation to operating power system networks, a temporary overvoltage may be defined as an overvoltage higher than the highest system voltage and lasting for more than 2 cycles. The representative temporary overvoltage is characterized by a standard short duration (1 min) power-frequency waveshape. TOVs may be classified according to whether the frequency of oscillation is lower, equal to or higher than the working voltage frequency. The causes that lead to temporary ovevoltages are many; the most frequent are summarized below (German & Haddad, 2004; Irwin & Ryan, 2001; Glavitsch, 1980).

**Faults to earth**: Phase-to-earth faults produce power-frequency, phase-to-earth overvoltages on the unfaulted phases. An overvoltage due to an insulation fault occurs on a three-phase network when the neutral is unearthed or impedance-earthed. The overvoltage magnitude depends on the system earthing and on the fault location. In effectively earthed systems, the temporary overvoltage is about 1.3 pu and the duration of the overvoltage, including fault clearing, is generally less than 1 s. In resonant earthed systems the temporary overvoltage is about 1.73 pu or greater and, with fault clearing, the duration is generally less than 10 s. Depending on the system configuration, separated portions of the system may become unearthed during fault clearing, and high overvoltages can be produced in the separated part.

Load rejection: Overvoltages caused by load rejection are a function of the rejected load, the system topology after disconnection, and the characteristics of the sources (e.g., speed and voltage regulators of generators). In a symmetrical three-phase power system the same relative overvoltages occur phase-to-earth and phase-to-phase. The longitudinal temporary overvoltages depend on whether phase opposition is possible; such phase opposition can occur when the voltages on each side of the open switching device are not synchronized. A distinction should be made between various system configurations when large loads are rejected. A system with relatively short lines and high short circuit power at terminal stations will have low overvoltages. A system with long lines and low short circuit power at generating sites will have high overvoltages. Load rejection can, on long uncompensated transmission lines, produce voltages of up 1.2 pu due to the *Ferranti* effect, at the substation end of the line which is disconnected from the source (i.e. remote end). Temporary overvoltages due to the Ferranti effect and load rejection are limited by shunt reactors, but because these shunt reactors remain connected to the system under normal working conditions, a problem of reactive power consumption is raised. Thyristor-controlled reactive compensation and shunt reactors with flat magnetizing characteristics have also been used.

**Resonance and ferro-resonance**: Temporary overvoltages may arise from the interaction of capacitive elements (lines, cables, series capacitors) and inductive elements (transformers, shunt reactors). The resonant overvoltage is initiated by a sudden change in the system configuration (e.g., switching of a transformer terminated line, isolation of a bus potential transformer through breaker capacitance). Ferro-resonance may occur when an operation (circuit opening or closing) is performed on the

network with a device having poles either separate or with no simultaneous operation. To avoid ferro-resonant conditions design modifications may be considered or steps can be taken to avoid the switching operations that cause them or to minimize the duration by selection of an appropriate protection scheme. Resonant and ferro-resonant overvoltages can have magnitudes greater than 2.0 pu and last until the condition is cleared. Parallel line resonance can occur during de-energization of one circuit of a double circuit transmission line with shunt reactive compensation. The energized line feeds the resonance condition through the inter-circuit capacitance. Voltages as high as 1.5 pu have been recorded on 420 kV systems. This voltage will remain until the line is re-energized or until the compensating reactor is switched out.

Temporary overvoltages are used to select surge arresters; that is, arresters are selected to withstand these overvoltages, which are not limited. When the metal oxide gapless surge arrester is not properly selected from the expected temporary overvoltages, it results in a considerable increase in the resistive component of leakage current in the arresters, and consequently in a temperature rise within the surge arrester and the possibility, if left long enough, of arrester failure. Resonant and ferro-resonant overvoltages are an exception and they should not be used for arrester selection, instead they should be limited by detuning the system from the resonant frequency, by changing the system configuration, or by installing damping resistors.

## 2.3. Slow-front Overvoltages

Sudden changes in electrical network structure give rise to transient phenomena that may result in overvoltages of aperiodic or oscillating type with rapid damping. Slow-front overvoltages are generally caused by switching operations (line and cable energization, faults and fault clearing, load rejections, switching of capacitive or inductive currents). These overvoltages may have times-to-crest of hundreds of microseconds and tail duration of thousands of microseconds. Switching surges have in practice a decaying oscillatory component superimposed on the power-frequency waveshape. The most common causes of switching transient overvoltages are presented below (Hileman, 1999; Chowdhuri, 1996; IEC 60071-2, 1996; Lloyd & Zaffanella, 1982; Erche, 1980).

*Line/cable energization and reclosing*: A three-phase energization or reclosing of a line/cable may produce switching overvoltages on all three phases. The overvoltage generation depends on the circuit breaker, and its calculation has to consider trapped charges left on the phases in case of high-speed reclosing. In the worst case each switching operation produces three phase-to-earth and three phase-to-phase overvoltages. Two methods are in use for characterizing the overvoltage probability distribution function: the *case-peak method* (each switching operation contributes one value to the overvoltage distribution) and the *phase-peak method* (each operation contributes three crest values to the probability distribution). The longitudinal insulation between non-synchronous systems can be subject to energization overvoltages of one polarity at one terminal and the crest of the operating voltage of the other polarity at the other terminal; consequently, the longitudinal insulation. In synchronized systems, the highest switching overvoltage and the operating voltage have the same polarity, and the

longitudinal insulation is exposed to a lower overvoltage than the phase-to-earth insulation. Line/cable switching overvoltages may be limited through the use of: (a) preinsertion resistors on the circuit breakers; (b) controlled closing of the breaker, or (c) surge arresters. Pre-insertion resistors and controlled closings reduce the overvoltage along the entire line. Surge arresters only reduce the overvoltages close to the arresters. Within a substation, arrester separation effects may be neglected; i.e., the switching impulse voltage is approximately the same throughout the substation, and the arrester provides protection to all connected equipment. Surge arresters are usually installed phase-to-earth.

**Initiation and clearing of faults**: The most frequent fault on power systems is the phase-to-earth short circuit, which is often accompanied by an increase of neutral voltage. Reducing the ratio  $X_0/X_1$ , however, will limit significantly the overvoltage. Slow-front overvoltages can be produced during phase-to-earth fault initiation and clearing. These overvoltages are only between phase-to-earth. If the switching overvoltages for energizing and reclosing are controlled to below 2.0 pu, fault and fault clearing may produce higher overvoltages. A conservative estimate may assume that the maximum overvoltage during fault clearing is about 2.0 pu, and the maximum value caused by a fault initiation is about (2k-1) pu, where k is the earth fault factor in per unit of the peak phase-to-earth system voltage.

*Load rejection*: Load rejection may increase longitudinal voltage stresses across switching devices, the phase-to-earth insulator stress and the energy discharged through the arresters. If the arresters are used to limit energization and reclosing overvoltages to below 2 pu, the energy dissipation in the arresters should be studied, especially when generators, transformers, long transmission lines, or series capacitors are present.

*Making and breaking of small inductive currents*: Several phenomena may be considered (Fulchiron, 1995; Martinez-Velasco & Popov, 2009).

- *Current chopping*: When interrupting small inductive currents, a premature interruption may occur with the current forced to zero before the natural current zero. The high *di/dt* associated with current chopping results in high induced voltage in the inductive circuit. This type of operation produces overvoltages of 2 to 3 pu in modern transformers; however, with transformers loaded with shunt reactors, values up to 5 pu may be reached which necessitates the use of surge arresters for protection.
- *Restrike*: This may occur when the current chopping phenomenon causes a voltage between the terminals that the circuit-breaker is unable to withstand. Multiple restrike then occurs until it is stopped by an increasing contact clearance. This phenomenon is characterized by high frequency wave trains of increasing amplitude and can present a considerable risk for equipment windings.
- *Prestrike*: When a device closes there can be a moment when the dielectric withstand between contacts is less than the applied voltage. An arc is then created between the contacts, and a voltage pulse is originated due to the sudden voltage cancellation. This pulse may result, due the circuit parameters and reflections, in the appearance of high frequency currents. If device operation is slow, the arcing current may be forced to zero. Arc extinction will then result in behavior similar to

that of the previous phenomenon. However, since dielectric withstand between contacts decreases with closing, the successive overvoltages decrease right up to complete closing. This phenomenon is very complex, and the resulting overvoltages depend, among other factors, on circuit-breaker characteristics, and configuration and parameters of the system.

*Switching of capacitive currents*: The list of scenarios may include the interruption of small capacitive currents, the energization of capacitor banks, and the energization of unloaded lines and cables (Fulchiron, 1995).

- *Breaking of capacitive circuits*: This operation normally presents few difficulties. Since capacitances remain charged at power-frequency wave peak value after the arc is extinguished at current zero, voltage is resumed at the equipment terminals with no transients. However, half-cycle after breaking, the device is subjected to a voltage that doubles the rated peak voltage. If it is unable to withstand this stress, reignition may occur. This is followed, provided the circuit so allows (single-phase or connected neutral circuit), by voltage inversion at capacitor terminals, raising them to a maximum load of three times peak voltage. The current breaks yet again and a new reignition may take place with a value five times peak voltage at the next alternation. Such behavior may result in considerable voltage escalation and must be avoided by choosing reignition-free equipment.
- Energizing of capacitor banks: When unloaded capacitor banks are energized by • means of slow operating devices, prestrike may occur between the contacts around the power-frequency wave peak. The frequency of the resulting oscillation is in general much higher than power frequency, and voltage oscillation is mainly centered on the power-frequency wave peak value. The maximum voltage value observed is about twice the power-frequency wave peak value. In the case of faster operating devices, arcing does not systematically occur around the peak value, and the transient voltage, if any, is thus lower. If a capacitor bank is reconnected soon after it has been disconnected from the network (i.e., its residual load voltage is between zero and the power-frequency wave peak voltage), the prestrike may occur around a peak of opposite polarity (i.e., breakdown under a stress twice peak voltage). Then, the maximum voltage may then be close to three times the power-frequency peak voltage. For safety reasons, capacitor banks are usually fitted with discharging resistors able to damp residual voltages with time constants of around one minute.
- *Energizing of unloaded lines and cables*: Slow closing of a device on this type of load may cause prestrike around the power-frequency wave peak. The voltage step applied to one end of the line or cable will spread and be reflected on the open end. Superimposition of the incident step and the reflected step results in a voltage stress about twice the applied step. This phenomenon must be taken into consideration particularly in EHV transmission lines, as a result of the small relative difference between operating voltage and insulating voltage.

The magnitude of switching surges is dependent on many factors including transmission line length and impedance, the degree and location of compensation, the circuit breaker characteristics, the feeding source configuration and the existence of trapped charge from prior energization of the transmission line. Many techniques have been developed to reduce the peak value of switching transients to less than 2 pu. Among these techniques are: switching resistors, controlled synchronized closing of circuit breakers, shunt reactors, drainage of trapped charges before reclosing by provision of leak resistors. In addition, protective measures, such as surge protection capacitors and surge arresters, are adopted. Modern metal oxide surge arresters are particularly efficient for such duties because of their fast switching response, energy absorption capability and excellent voltage–current non-linearity. Developments in controlled point-on-wave (POW) switching have introduced microprocessor-based technology for circuit-breaker operation control (CIGRE WG A3.07, 2004). This can be very effective, particularly when used in conjunction with metal oxide surge arresters for transmission line overvoltage control. Corona losses and earth return attenuation have, however, little effect on reducing switching surge overvoltages except on long transmission lines.

## **2.4. Fast-front Overvoltages**

They are generally produced by lightning discharges, although switching of nearby equipment may also produce fast-front waveshapes (Hileman, 1999; Chowdhuri, 1996; IEC 60071-1, 2010; IEEE Std C62.82.1; 2010; CIGRE WG 33-01, 1991; Berger, 1990; Anderson, 1987). Their time to peak value may vary between 0.1 and 20 µs.

*Fast-front switching overvoltages*: The connection or disconnection of nearby equipment can produce oscillatory short duration fast rising surges with similar waveshapes to lightning. The insulation strength for this waveshape is closer to that of the standard lightning impulse than that of the standard switching impulse. Arresters cannot limit these very steep front surges. However, as their magnitudes usually are smaller than those caused by lightning, their importance is restricted to special cases. Their maximum value is approximately 3.0 pu with restrike and 2.0 pu without restrike.

*Fast-front lightning overvoltages*: Lightning overvoltages are characterized by very high peak currents and relatively low energy content. They can be estimated by assuming that the return stroke current is an aperiodic wave. From the point of view of power system overvoltages, the important parameters of the lightning stroke are the peak current value, the front time (or time-to-crest) and the tail time (or time-to-half-value). All of them are statistically distributed. Field measurements have shown that the mean value of peak current is about 30 kA with typical front times of 2  $\mu$ s. The rising front of lightning strokes are generally of negative polarity (negative cloud and positive earth), and roughly 10 % have positive polarity.

Lightning can affect overhead lines in three ways: (i) a direct stroke on a phase conductor; (ii) a direct stroke to earth wire or a tower top when lightning hits a shielded line; (iii) an induced voltage when the lightning stroke occurs to earth in the vicinity of the line. Induced voltages by nearby strokes hardly exceed 300 kV and are important only for lower (distribution) voltage systems.

Lightning surges travel along the line and may cause internal breakdown of terminal equipment system insulation. As these surges travel from the stroke terminating point to the station, corona decreases both the front steepness and the crest magnitude. The

voltage wave front arriving at the substation can be significantly affected by the line termination, although in the case of a cable termination, the wave front may be drastically reduced. Protection against lightning overvoltages is usually based on the most probable lightning current shape which might hit the system and the keraunic level or density of lightning flashes (flashes per kilometer square per year) in the location area of the system.

*Direct stroke to phase conductors*: Most transmission line towers are equipped with shielding earthed wires, whose purpose is to divert the lightning stroke away from the phase wire and thus provide shielding. Any lightning stroke that penetrates the shield is termed a shielding failure. For insulation co-ordination purposes, the direct stroke may not require further investigation if the transmission line is effectively shielded.

Direct stroke to earth wires: A backflashover can occur when an earth wire, either at a tower or at a point midway between two towers, is struck by lightning. In any case the lightning stroke current travels to earth via the tower causing a voltage difference between the tower cross arms and the line conductors. The magnitude of the stroke current can vary from a few kA to over 200 kA. The combination of earth wire and tower surge impedances with the lightning current will produce a voltage at the tower top which is oscillatory due to successive reflections from the tower base, and dependent on the earthing impedance. Not all of the tower top voltage will appear across the line insulator because there is some reduction due to the position of the insulator on the cross-arm and also voltage will be mutually coupled from the shield wire to the phase conductor. So the voltage that appears across the line insulator will be similar but marginally smaller than the tower top voltage. Depending on the V-t characteristics of the line insulation, the backflashover may occur near the peak of the voltage pulse or on the surge tail. From 750 kV up, there is virtually no risk of backflashover, which justifies the installation of earth wires on EHV lines. Below 90 kV, these wires provide efficient protection only when the tower footing is excellent (i.e., low-value impedance).

*Indirect lightning strokes*: Indirect strokes are more frequent than direct ones and may be even more dangerous than direct strokes for distribution-level overhead lines. If lightning falls next to the line, the energy flowing off to the earth causes a very fast variation of the electromagnetic field. The waves induced on the line are similar in shape and amplitude to those obtained by direct lightning. They are mainly characterized by a very steep front (around one micro-second) and their very fast damping. When the voltage wave resulting from a lightning stroke reaches a MV/LV transformer, voltage transfer mainly occurs by capacitive coupling. The amplitude of the overvoltage transmitted to the secondary winding (e.g., the LV side) is less than 10 % of its value on the primary winding (e.g., the MV side), generally less than 70 kV.

*Lightning overvoltages entering substations*: The magnitude and rate of rise of overvoltages due to lightning strokes on transmission lines is an important consideration for substation insulation design. Having determined the insulation required for the line, it is usual to find that the lightning withstand level is in excess of commercially available lightning strength levels of the substation equipment. Thus, unless precautions are taken, overvoltages entering the station can cause insulation failure.

On the other hand, it is important to account for corona effect. As the lightning surge travels towards the substation from the struck point the wave front above the corona inception voltage will be retarded by corona loss. Skin effect on the line conductors will cause further attenuation due to the high frequency nature of the surge. It is usual to consider lightning strokes that occur within only a few kilometers to the substation when assessing surge arrester requirements and the associated risk of failure of the substation.

The voltage arriving at the substation can be evaluated from the lightning performance of the incoming lines and compared with the lightning withstand level for the substation equipment (Hileman, 1999). For well shielded transmission lines, the backflashover condition, close to the substation, is of prime concern for determining the location and number of surge arresters required to achieve insulation co-ordination of the substation for lightning surges. The risk of a backflashover can be reduced by keeping tower footing impedances to a minimum, particularly close to the substation (first five to seven towers). The terminal tower is usually bonded to the substation earth mat and will have very low earthing impedance (1 ohm). However, the procedure for gapping down on the first three or four towers where line coordinating gaps are reduced in an attempt to reduce incoming voltage surges will increase the risk of backflashover.

The open-circuit-breaker condition is a scenario to be studied, since if the line circuitbreaker is open the surge voltage will double-up at the open terminal. Various levels of stroke current can be simulated at different tower locations and the resultant substation overvoltages can be assessed.

If it is considered that the lightning withstand level of the substation will be exceeded or that there is insufficient margin between the calculated surge levels and the lightning withstand level to produce an acceptable risk, then surge arrester protection must be applied. Surge arresters can be situated at the line entrance but consideration must be given to the voltage profile as the surge travels through the substation. The rating of the MO surge arresters has to be assessed from TOV requirements. The protective level of the arrester and the safety factor for a given system configuration can be assessed from detailed computer simulation (Martinez-Velasco & Castro-Aranda, 2009). IEC 60071 recommends a safety factor of 1.25 for 420-kV equipment. The surge arrester current calculated for this condition should be the worst case and can therefore be used to assess the nominal discharge current requirement of the surge arrester (i.e., 5 kA, 10 kA or 20 kA). To make full use of the MO surge arresters protective level, the arrester should be placed as close as possible to the equipment being protected. In the case of the open line circuit-breaker this may well be 10-20 m distance. Due to this separation, and depending on the rate of rise of the surge voltage, a voltage greater than the residual voltage at the surge arrester location will be experienced at the terminals of the opencircuit-breaker. This must be taken into account when assessing the substation overvoltage since additional surge arresters may be required because of the distances involved in the layout of the substation. It then follows that surge arresters have a protective distance which is sensitive to the rate of rise of the incoming surge voltage (Hileman, 1999), and this must be taken into consideration when assessing the lighting overvoltage on equipment remote from the surge arrester.

#### 2.5. Very fast-front Overvoltages

Very fast-front transients belong to the highest frequency range of transients in power systems (from 100 kHz up to 50 MHz). Their shape is usually unidirectional with time to peak below 0.1  $\mu$ s, total duration below 3 ms, and with superimposed oscillations at frequencies below 100 MHz. Causes that can originate these overvoltages are disconnector operations and faults within gas insulated substations (GIS), switching of motors and transformers with short connections to the switchgear, and certain lightning conditions (Ecklin, Schlicht, & Plessl, 1980; Martinez-Velasco, 2007).

Very fast-front transient overvoltages in GIS are of greater concern at the highest voltages, for which the ratio of the insulation level to the system voltage is lower. Some equipment failures and arcing problems between earthed parts have occurred at system voltages above 420 kV; they have been correlated with disconnect switch and circuit breaker operation.

The generation and propagation of very fast-front transients from their original location throughout a GIS can produce internal and external overvoltages. The main concern is internal overvoltages between the centre conductor and the enclosure. However, external transients can be dangerous for secondary and adjacent equipment. The external transients include transient voltages between the enclosure and earth at GIS-air interfaces, voltages across insulating spacers in the vicinity of GIS current transformers, when they do not have a metallic screen on the outside surface, voltages on the secondary terminals of GIS instrument transformers, and radiated electromagnetic fields, which can be dangerous to adjacent control or relay equipment.

#### 3. Surge Arresters

#### **3.1. Introduction**

Surge arresters are connected across an apparatus to provide a low-resistance path and to limit the various types of transient voltages below the corresponding insulation level of the apparatus. A surge arrester should act like an open circuit during normal operation of the system, limit transient voltages to a safe level and bring the system back to its normal operational mode as soon as the transient voltages are suppressed (Chowdhuri, 1996). A surge arrester must have an extremely high resistance during normal system operation and a relatively low resistance during transient overvoltages; that is, its voltage - current (V-I) characteristic must be non-linear.

There are two main types of surge arresters: the expulsion type and the valve type. Expulsion arresters are still in use, but they are no longer manufactured, so they are not reviewed here.

Valve arresters consist of nonlinear resistors which act like valves when voltages are applied to them. There are two types of valve arresters: silicon carbide (SiC) and metal oxide (MO). SiC surge arresters use spark gaps connected in series with discs made with a non-linear SiC material. The spark gaps provide the high impedance during normal conditions while the SiC discs impede the flow of current following sparkover.

The V-I characteristic of SiC-type surge arresters are a combination of both the SiC disc and the gap behavior. The MO varistor material used in modern high voltage gapless surge arresters has a highly non-linear V-I characteristic. Varistors are made up of zinc oxide (ZnO) powder and traces of oxides of other metals bound in a ceramic mould. Their characteristic avoids the need for series spark gaps. Therefore, the electrical behavior is determined solely by the properties of the MO blocks.

The V-I characteristic of both SiC and ZnO valve elements are shown in Figure 1. Note the difference between leakage currents in both valve types for a given voltage. The series gap is essential for a SiC valve arrester to prevent thermal runaway during normal operation, while gapless operation is possible with ZnO arresters because of the low leakage current during normal operation.

Both types of arresters are reviewed below, but the rest of the section is dedicated to the MO surge arrester, since it is the most common type that is presently installed (Hileman, 1999; Martinez-Velasco & Castro-Aranda, 2007). IEEE standards for surge arresters are C62, which define tests and ratings, and provide applications guides (IEEE Std C62.1, 1989; IEEE Std C62.2, 1987; IEEE Std C62.11, 2005; IEEE Std C62.22, 2009). IEC standards for high voltage (> 1 kV) surge arresters are denoted 60099 (IEC Std 60099-1, 1999; IEC Std 60099-3, 1990; IEC Std 60099-4, 2009; IEC Std 60099-5, 2000; IEC Std 60099-6, 2002).



#### **3.2. Valve Type Arresters**

#### **3.2.1. Gapped Silicon Carbide Arresters**

SiC gapped arresters consist of series spark gaps with series blocks of nonlinear resistors which act as current limiters. The current-limiting block has nonlinear resistance characteristics. The nonlinear resistors are built from powdered SiC mixed with a binding material, moulded into a circular disc and baked. The disc diameter depends on its energy rating, and the thickness on its voltage rating. The V-I

characteristic of a SiC nonlinear valve block has a hysteresis-type loop, being the resistance higher during the rising part of the impulse current than during the tail of the current wave. The nonlinear properties are due to the resistance-temperature properties of the junction between SiC crystals. The function of the air gap is to isolate the current limiting block from the power-frequency voltage under normal operating conditions. Without a gap, a power-frequency leakage current would constantly flow through the valve block, which would overheat the block, and could eventually lead to thermal runaway.

The series gap sparks over if the magnitude of the applied voltage exceeds a preset level. The sparkover voltage depends upon the voltage waveshape: the steeper the voltage rise, the higher the sparkover voltage. Once the energy in the transient voltage is dissipated, power-follow current will flow through the valve elements. A relatively high current will continue to flow through the arrester, after sparkover and after the overvoltage has gone down, if the power voltage across the arrester is high enough, since the gap arc has a low resistance and the current is primarily determined by the V-I characteristic of the SiC block. The voltage drop across the valves rises with the discharge current that flows through them. However, due to the nonlinearity of the valve blocks, the flow of current will be so low that the arc across the series gap elements will become unstable and be quenched, thus isolating the power-frequency source from the arrester. Take into account that the sparkover and the discharge voltage are not equal. To ensure arc extinction and resealing, a mechanism is provided for the control of the arc. An important effect of this control is that for fast transients almost the entire voltage appears across the current-limiting block.

# 3.2.2. Gapless Metal Oxide Arresters

An MO varistor consists of highly conductive particles of MO, usually ZnO, suspended in a semiconducting material. The manufacturing process determines the size of the MO particles as well as the thickness and resistivity of the semiconducting material. In a gapless arrester the MO block is continuously subjected to the power-frequency voltage, but the power-frequency leakage current through an MO arrester is so small that there is no danger of a thermal runaway. The voltage-current characteristic of a MO surge arrester exhibits a knee for small currents (in the milliampere region). The V-I characteristic of a MO block in the protection region (high current flow) is insensitive to the temperature of the block, but the V-I characteristic near the knee is temperaturesensitive, see Figure 1. For an applied voltage near nominal, the electric current through the arrester is mostly capacitive and the low value on the order of a milliampere. As the voltage increases, the current increases much faster. The increase of the current occurs in the component which is in phase with the voltage while the capacitive component remains constant. The arrester discharge voltage for a given current magnitude is directly proportional to the height of the valve element stack and is more or less proportional to the arrester rated voltage. The operation of an arrester is sensitive to the rate of rise of the incoming surge current: the higher the rate of rise of the current, the more the arrester limiting voltage rises. The instantaneous temperature and resistance of a valve block is a function of the energy dissipated in the block up to that instant. However, the energy dissipated in a valve block for any specific current level on the front of the current wave is smaller for a faster rising current than that for a slower rising current at the same current level. Then, the instantaneous resistance of a valve block will be higher for a faster rising current than for a slower rising current. Hence, the discharge voltage for a faster rising current will be higher.

#### **3.2.3. Gapped Metal Oxide Arresters**

The MO arrester has several advantages in comparison with the SiC arrester (simplicity of design, decreased protective characteristics, increased energy absorption capability); however, the power-frequency voltage is continuously resident across the MO. High currents can result from TOVs and produce heating; if the TOVs are sufficiently large in magnitude and long in duration, temperatures may increase sufficiently to cause thermal runaway and failure. In addition, the discharge voltage increases as the arrester discharge current increases. The performance of MO blocks at higher discharge currents can be improved by equipping them with a shunt gap designed to spark over whenever the discharge current through the arrester exceeds a certain value; e.g. 10 kA. Some distribution-class arresters use series gaps that are shunted by a linear component impedance network.

# 3.3. Characterization of Metal Oxide Surge Arresters

# 3.3.1. Arrester Characterization

Some information (voltage ratings, class or discharge current, frequency) is needed for identification of a MO surge arrester. These values are obtained from tests established and detailed in standards. IEC standards classify arresters according to the nominal discharge current and line discharge class. Discharge current and discharge class cannot be selected independently of each other (Hileman, 1999). IEEE standards classify arresters into three primary *durability* or *capability* classes (IEEE Std C62.2, 1987): (1) *station*, used primarily in HV and EHV systems; (2) *intermediate*, used between station and distribution; and (3) *distribution*, used in distribution systems, and further divided into *heavy duty, normal duty* and *light duty*.

While in service a MO surge arrester must withstand the maximum rms value of powerfrequency voltage that may appear across its terminals and be capable of operating under the maximum TOV that can occur at its location during the length of time that such overvoltage will exist. In addition, the arrester should have an energy capability greater than the energy associated with the expected switching surges on the system.

The ratings of a MO surge arrester in the IEC Application Guide are the continuous operating voltage (COV), the rated voltage (TOV capability at 10 seconds), the nominal discharge current, the line discharge class, and the pressure relief class (IEC Std 60099-5, 2000). The nominal discharge current is selected by calculation or estimation of the lightning current discharge by the arrester. The line discharge class is selected by comparison of the arrester energy capability with the energy discharge required. The pressure relief class is selected by comparison to the system fault current.

The selection of a MO arrester according to the IEEE standard is based on similar information (IEEE Std C62.22, 2009). The IEC rated voltage is similar to the IEEE

duty-cycle voltage except that in IEEE this voltage is not defined in terms of the TOV capability. Therefore, to determine arrester ratings, the following rules are to be considered:

- 1. The steady-state voltage that the arrester can support indefinitely, known as the *maximum continuous operating voltage* (MCOV) in IEEE and *continuous operating voltage* (COV) in IEC, must be equal to or greater than the maximum phase-to-earth system voltage.
- 2. The temporary overvoltage across the arrester must be less than the arrester TOV capability.
- 3. Switching surge energy discharged by the arrester must be less than the energy capability.
- 4. The pressure relief current must be equal to or greater than the fault current.

Each class and type of arrester is subjected to a series of tests, which may be divided between those that serve to define the arrester ability to protect itself (durability/capability) and those that define the arrester ability to protect the equipment to which it is applied (protective characteristics). In addition, manufacturers provide energy capabilities to define the arrester ability to discharge the energy in a switching surge or a lightning discharge. Tests to establish these energies are not yet included in standards.

# **3.3.2.** Protective Characteristics

The purpose of the discharge-voltage characteristic tests is to verify the voltage level appearing across an arrester under specific surge conditions. The protective characteristics are voltages across the arrester for a specified discharge current magnitude and shape. Both IEC and IEEE standards identify three characteristics tests whose objectives are to determine the following voltages (IEEE Std C62.11, 2005; IEC Std 60099-4, 2009):

- 1. Steep current impulse discharge voltage: This voltage is known as front-of-wave protective level (FOW) in IEEE. In the IEC standard, it is the discharge voltage obtained by discharging a current having a 1- $\mu$ s front and a crest current equal to the nominal discharge current. According to the IEEE standard, it is the voltage across the arrester having a time-to-crest of 0.5  $\mu$ s when discharging the lightning impulse current. This discharge voltage is obtained by using different times to crest (usually 1, 2, and 3  $\mu$ s) and plotting the voltage as a function of the time to crest of the voltage.
- 2. Lightning impulse protection level (LPL): It is the highest of the discharge voltages obtained across the arrester for arrester discharge currents having an 8/20 µs waveshape and crest magnitudes equal to 0.5, 1.0, and 2.0 times the nominal discharge current in IEC, or values of 1.5, 3.0, 5, 10, and 20 kA in IEEE. For arresters applicable to 500-kV systems, IEEE also specifies the 15-kA discharge. Manufacturers may also provide the 40-kA discharge voltage.
- 3. Switching impulse protection level (SPL): This is the voltage across the arrester when discharging a current impulse with a front greater than 30  $\mu$ s and a tail less

than 100  $\mu$ s in IEC standard, or having a 45- to 60- $\mu$ s time-to-crest in IEEE standard. This test is not required for distribution arresters.

The discharge voltage magnitude and time-to-crest are functions of the time-to-crest and magnitude of the discharge current; see Figure 2.



Figure 2. Effect of time-to-crest of arrester current.

#### **3.3.3. Energy Capabilities**

The energy that an arrester can absorb during an overvoltage is known as *energy withstand capability*. This capability is often expressed in terms of kJ per kV of arrester COV/MCOV or per kV of duty-cycle rating. Because it is dependent on the specific form (magnitude, waveshape and duration) of the overvoltage, the energy handling capability cannot be expressed by a single value of kJ/kV. Manufacturers typically publish some information on energy handling capability, but there are no standardized tests to determine the energy handling capability of arresters.

The switching surge energy capability is of importance when selecting the arrester ratings; on the other hand, with the increased use of arresters for protection of transmission and distribution lines, the energy capability in the lightning region is also essential.

The capability of discharging the energy contained in a switching surge is partially determined by the low-current, long-duration test. This energy is the energy from multiple discharges, distributed over one minute, in which the arrester current is less than a specified magnitude. Thus it becomes evident that the energy capability depends on the rate at which energy is discharged by the arrester.

Some reports have shown that when arresters are tested until failure, the energy capability exhibits a probabilistic behavior (Hileman, 1999). Assuming that the Weibull cumulative distribution function can be used to model the energy characteristic and setting the discharge energy for the standard tests at the mean minus 4 standard deviations, the probability of arrester failure is given by the following equations:

$$P_{\rm F} = 1 - 0.5 \left(\frac{Z}{4} + 1\right)^5 \tag{1}$$

where

$$Z = \frac{W_{\rm C} - \mu}{\sigma} = \frac{\left(W_{\rm C} / W_{\rm R}\right) - 2.5}{0.375}$$
(2)

where  $\mu$  is the average or mean energy capability,  $\sigma$  is the standard deviation,  $W_{\rm C}$  the energy capability, and  $W_{\rm R}$  the rated energy from the standard tests; i.e., that provided by the manufacturer. The equation for Z assumes a standard deviation of 15% of the mean.

Some simple approaches can be applied to estimate the energy discharged by a surge arrester. An accurate quantification of the energy discharge may be obtained through time-domain simulation.

#### 3.3.4. Metal Oxide Surge Arrester Characteristics

The nonlinear V-I characteristic of an arrester valve (SiC or ZnO) is given by:

$$I = kV^{\alpha}$$

The parameter k depends upon the dimensions of the valve block, while  $\alpha$ , which describes the nonlinear characteristic, depends upon the valve-block material. For a SiC block,  $\alpha$  is typically 5, whereas for a ZnO block  $\alpha$  is greater than 30.

The V-I characteristic of MO arresters can be divided into three regions (see Figure 3) (Hileman, 1999):

- 1. In region 1, *I* is less than 1 mA and is primarily capacitive.
- 2. In region 2, *I* is from 1 mA to about 1000 or 2000 A and is primarily a resistive current.
- 3. In region 3, *I* is from 1 to 100 kA. For very large currents, the characteristic approaches a linear relationship with voltage; i.e., the MO varistor becomes a pure resistor.

Coefficient  $\alpha$  is variable for MO varistors, reaching a maximum of about 50 in the first region and decreasing to about 7 to 10 in the third region. Thus, for MO varistors,  $\alpha$  is primarily used to indicate the flatness of the characteristic and should not be employed to model the arrester. However, in some cases, it is convenient to use a  $\alpha$  value within a limited range to assess the arrester performance; e.g., the TOV capability of the arrester. The V-I characteristic depends upon the waveshape of the arrester current, with faster rise times resulting in higher peak voltages.



#### **3.4. Metal Oxide Surge Arresters Models**

The V-I characteristic of a surge arrester has several exponential segments (Dommel, 1986), and each segment can be approximated by the following formula:

$$i = p \left(\frac{v}{V_{\rm ref}}\right)^q \tag{4}$$

where q is the exponent, p is the multiplier for that segment, and  $V_{ref}$  is an arbitrary reference voltage that normalizes the equation.

The first segment can be approximated by a linear relationship to avoid numerical underflow and speed up the simulation. The resistance of this first segment should be very high since the surge arrester should have little effect on the steady-state solution of the network. The second segment is defined by the parameters p, q and  $V_{\min}$ , the minimum voltage for that segment. Multiple segments are typically used to enhance the accuracy of the model since the exponent decreases as the current level increases. Each segment has its own values for p, q and  $V_{\min}$ .

Manufacturers test each disc with a current pulse (typically a current pulse with a 10 kA peak) and record a reference voltage. The resulting peak voltage is the reference voltage  $V_{10}$ , the voltage at 10 kA for single column surge arrester. The V-I curves often use the  $V_{10}$  value as the 1.0 per unit value. The V-I curve can be determined by multiplying the per unit arrester voltages by the  $V_{10}$  for that rating.

The information required to construct an arrester model is (Martinez & Durbak, 2005): (i) a reference voltage proportional to the arrester rating (i.e.,  $V_{10}$ ); (ii) the number of parallel columns of discs; (iii) the V-I characteristic in per unit of the reference voltage. A supporting routine available in most transients programs allows users to convert the set of manufacturer's V-I points to a set of p, q and  $V_{\rm nin}$  values. A different curve should be created for each waveshape and manufacturing tolerance (maximum or minimum). The voltages are usually given in a per unit fashion where the reference voltage (1.0 pu) is either the voltage rating or  $V_{10}$ , the peak voltage for a 10 kA, 8/20 µs current wave.

The choice of arrester V-I characteristic depends upon the type of transient being simulated since current waveshapes with faster rise times will result in higher peak voltages.

*Models for low-frequency and slow-front transients*: To construct a surge arrester model for these frequency ranges, the information to be obtained from the manufacturer's literature is that listed above; that is, ratings and characteristics, as well as V-I curves. The arrester model is then edited using the supporting routine available in transients programs.

*Models for fast-front transients*: The previous surge arrester model does not incorporate time or frequency dependence. Actually, the surge arrester waveshapes would be skewed if they were physically measured in a laboratory, and the peak of the arrester voltage would occur before the peak of the current. For a given peak current, the peak voltage increases as the front time decreases. However, the percentage increase is only slightly proportional to the current magnitude. The fast front phenomenon appears to be an inductive effect, but it is not that of a simple linear inductance.

The dynamic performance of MO surge arresters was first described in late 70's. Since then several models have been developed to represent a frequency-dependent behavior. All these models incorporate a nonlinear resistor to account for the V-I characteristic of MO varistors, and an inductor to include frequency-dependent behavior.

One of the most popular MO surge arrester models is that adopted by IEEE, which is shown in Figure 4 (IEEE WG, 1992); it incorporates two time independent nonlinear resistors ( $A_0$  and  $A_1$ ), a pair of linear inductors ( $L_0$  and  $L_1$ ) paralleled by a pair of linear resistors ( $R_0$  and  $R_1$ ), and a capacitor C. The V-I characteristic of  $A_1$  is slightly less than the 8/20 µs curve while  $A_0$  is 20% to 30% higher.  $R_1$  and  $L_1$  form a low pass filter that sees a decaying voltage across it. A lumped inductance of about 1 µH per meter for the earth leads should also be included in series with the model. In transients simulations the nonlinear resistors should be modeled as exponential segments as described above. For low frequency surges, the impedance of the filter  $R_1$  and  $L_1$  is very low and  $A_0$  and  $A_1$  are practically in parallel. During high frequency transients, the impedance of the filter becomes very high and the discharge current is distributed between the two nonlinear branches. Figure 5 shows V-I characteristics of  $A_0$  and  $A_1$ , see also Table 1, where voltage values are in per unit of  $V_{10}$ .  $A_0$  is presented as 5 segments and  $A_1$  as 2 segments.



Figure 4. IEEE MO surge arrester model for fast-front surges.



Figure 5. V-I characteristics for nonlinear resistors (Martinez & Durbak, 2005) (© 2005 IEEE).

*			
	Current	Voltage (per unit of $V_{10}$ )	
	(kA)	$A_0$	$A_1$
	0.01	0.875	0.681
	1	1.056	0.856
	5	1.131	
	10	1.188	
	15	1.244	
	20	1.313	1.000

Table 1. Values for  $A_0$  and  $A_1$  in Figure 5 (Martinez & Durbak, 2005) (© 2005 IEEE)

The formulas to obtain the parameters of the circuit shown in Figure 4, initially suggested by Durbak (1985), are based on the height of the arrester, the number of columns of MO disks, and the curves shown in Figure 5.

The information required to determine the parameters of the fast-front model is as follows:

- d = height of the arrester, in meters
- n = number of parallel columns of MO disks
- $V_{10}$  = discharge voltage for a 10 kA, 8/20 µs current, in kV
- $V_{\rm ss}$  = switching surge discharge voltage for an associated switching surge current, in kV.

Linear parameters are derived from the following Eqs. (IEEE WG, 1992):

$$L_{0} = 0.2 \frac{d}{n} (\mu H) \qquad R_{0} = 100 \frac{d}{n} (\Omega)$$

$$L_{1} = 15 \frac{d}{n} (\mu H) \qquad R_{1} = 65 \frac{d}{n} (\Omega)$$

$$C = 100 \frac{n}{d} (pF)$$
(5a)
(5b)
(5c)

These formulas do not always give the best parameters, but provide a good starting point. The procedure proposed by the IEEE WG to estimate all parameters can be summarized as follows (IEEE WG, 1992):

- 1. Determine linear parameters  $(L_0, R_0, L_1, R_1, C)$  from the previously given formulas, and derive the nonlinear characteristics of  $A_0$  and  $A_1$ .
- 2. Adjust  $A_0$  and  $A_1$  to match the switching surge discharge voltage.
- 3. Adjust the value of  $L_1$  to match the  $V_{10}$  voltages.

A simplified version of the IEEE model was proposed by Pinceti & Giannettoni (1999), see Figure 6. According to the authors of this model, the capacitance in the model shown in Figure 4 can be eliminated, since its effect is negligible, and the two resistances in parallel with the inductances can be replaced by a single resistance R, of about 1 M $\Omega$ , placed between model terminals to avoid numerical problems.



Figure 6. Simplified MO surge arrester model for fast-front surges.

This model does not take into consideration any physical characteristic of the arrester and its operating principle is similar to that of the IEEE model:

- The definition of nonlinear resistors characteristics  $A_0$  and  $A_1$  is the same that for the IEEE model.
- The two inductances are calculated by means of the following equations:

$$L_{0} = \frac{1}{12} \cdot (K-1) \cdot V_{n} \quad (\mu H)$$

$$L_{1} = \frac{1}{4} \cdot (K-1) \cdot V_{n} \quad (\mu H)$$

$$K = \frac{V_{1/T2}}{V_{10}}$$

$$(6a)$$

$$(6b)$$

$$(7)$$

being  $V_n$  the arrester rated voltage (in kV),  $V_{10}$  the discharge voltage for a 10 kA, 8/20 µs current (in kV),  $V_{1/T2}$  the discharge voltage for a 10 kA steep current pulse (in kV). The decrease time  $T_2$  in  $V_{1/T2}$  is not specified since it can vary between 2 and 20 s and each manufacturer can choose the preferred value. The value  $V_{1/T2}$  is similar to the front-of-wave (FOW) discharge voltage defined in the IEEE standard (IEEE Std C62.22, 2009).

The model was refined in a later work (Caserza Magro, Giannettoni, & Pinceti, 2004). It was proved that whenever  $V_{1/T2}$  is not available and the factor *K* is more than 1.18, the inductance parameters can be estimated as follows:

$$L_0 = 0.01 \cdot V_n \ (\mu H)$$
 (8a)

$$L_1 = 0.03 \cdot V_n \ (\mu H)$$
 (8b)

*Models for very fast-front transients*: Basically, the recommended models are similar to those proposed for modeling surge arresters in fast-front surge simulations, but representing frequency dependent behavior by means of a distributed-parameter lossless line.

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