VERY-LARGE-SCALE INTEGRATION OF ELECTRONIC CIRCUITS

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Contents

Summary

This chapter aims to offer the reader a comprehensive view about what we understand nowadays under the term VLSI. Within the Introduction, a historical perspective is given first, describing how the term has evolved from integrated circuits with hundred thousand transistors to integrated systems in the range of billions of devices including on-chip or on-package sensors. Then, the main topics having an influence on the conception, design and implementation of VLSI are introduced and structured into four main categories to be considered in depth in subsequent sections.

Section 2 deals with architectural issues, describing these for both general-purpose and DSP digital systems, putting an emphasis on the coexistence with analog, mixed-signal and RF components as in use in many present applications. Section 3 addresses the level of circuit design, bringing to the foreground the limitations having an impact like complexity, power, clocking, digital-analog coexistence, modeling, etc.

Section 4 is oriented to discuss the evolution of MOS technologies, the advantages and inconveniences that the new technological nodes present as well as to introduce the fabrication techniques in use for advanced processes. A glimpse on sensing devices compatible with nanometric MOS technologies is also given, with the aim of offering a flavor of what can be achieved either now or in the near future combining MOS and

sensors on the same substrate or in the same package. Section 5 intends to review the different auxiliary techniques required to design and implement VLSI. Attention is paid to CAD tools and test methodologies as well as how to integrate these techniques into a design and fabrication flow which allows the designers to afford their job with a reasonable guarantee of success. Finally, some general conclusions are drawn in a closing Section.

1. Introduction

The concept of Very-Large-Scale Integration (VLSI) was coined more than thirty years ago to describe the process of conceiving, designing and fabricating integrated circuits by combining thousands of transistors and their interconnections in a single chip. This happened when the available MOS technologies had a feature size larger than 1 μm. As technology evolved toward smaller sizes, decreasing more and more, the term VLSI was applied to chips formed by hundreds of thousands and even hundreds of millions of transistors. Since then, the minimum dimensions have been shrinking down even more as we handle today billions of transistors [1].

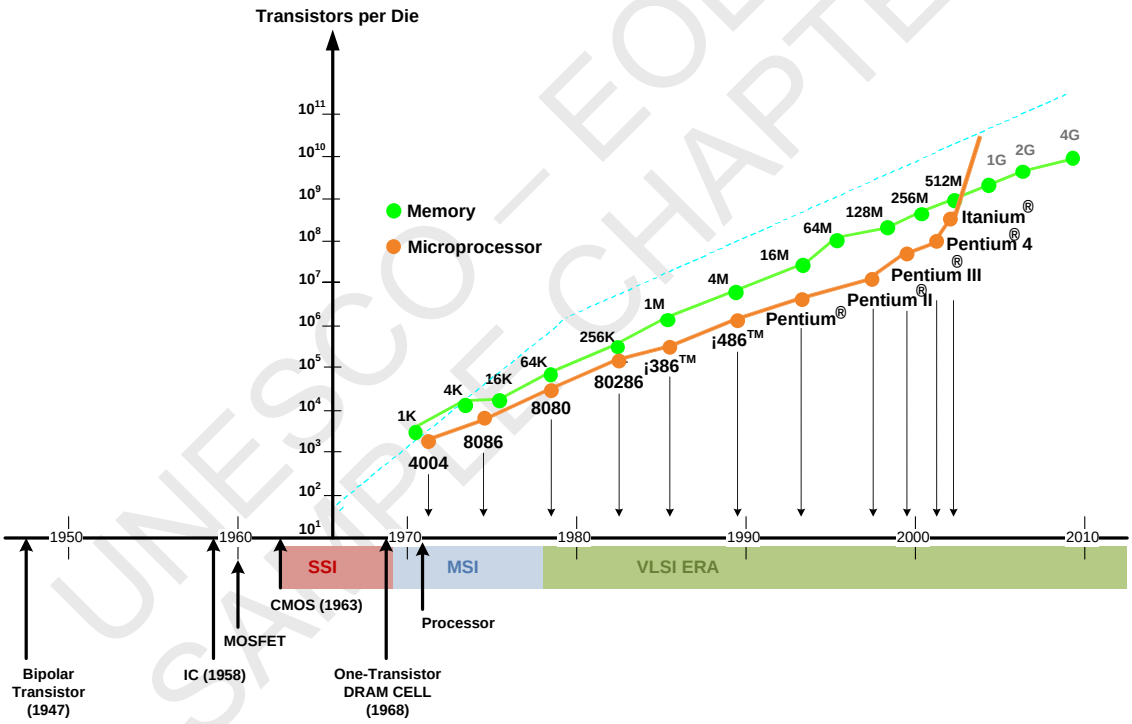

Figure 1. Milestones in Microelectronic Technologies and Moore's Law

Historically, the first integrated circuits consisted only of a few components, making it possible to fabricate one or more logic gates on a single device, in what is now retrospectively known as Small-Scale Integration (SSI). Afterwards, further improvements in technology led to chips with hundreds of logic gates, the so-called Medium-Scale Integration (MSI), and even more than thousand logic gates (large-scale integration or LSI). Then, it comes up the definition of VLSI attached to integrated circuits approaching one hundred thousand devices. In the past, as current technology

moves far away these numbers, there was an effort to name and define other levels of large-scale integration, like Ultra-Large-Scale Integration (ULSI); but this trial was abandoned due to the fast pace in reducing sizes and increasing complexity and the volatility of any definition. An empirical law, the well-known "Moore Law" [2], states that the density of transistor in a chip doubles approximately every 18 months. This law has been empirically demonstrated since has been fulfilled as can be seen in Figure 1, which reflects that principle in terms of INTEL's microprocessor and memory evolution. Microprocessors and memories have defined the two traditional niches for VLSI systems since they have benefited from such a fast evolution.

Thus, present MOS technologies provide chips with many billions of transistors and there is no forecast on the limits to be reached as current generation processes move from 65 and 45 nm to generations in the proximity of 10 nm and beyond. This continuous movement toward smaller dimensions is what nowadays is known as "More Moore" tendency in the evolution of integration, as it is foreseen that there are still room to continue with the reduction of dimensions for the next decade or so. In this sense, we can define a coordinate which has been primarily determining the different generations of VLSI circuits, namely the device dimensions. Figure 2-a aims to give the flavor of such evolution representing the present trends referred to the technology nodes as are defined today. Vertical axis is indicating how size is been shrunk. The upper clouds indicate which have been the baseline circuits (microprocessors and memories) and the one to the left indicates that probably after reaching the scaling limits for CMOS, this evolution will continue supported by new devices beyond CMOS.

On the other hand, there is another tendency governing the evolution of integrated circuits and systems nowadays, the so-called "More than Moore" tendency. It is due to the need of incorporating non-digital devices into a chip since new application fields are demanding the usage of analog circuits, sensors and/or actuators within the same semiconductor substrate. This requires several changes in the design flow of complex ICs and poses as well new problems to be solved. Figure 2-b intends to present an overview of this emerging tendency. As can be seen from that Figure, non-digital devices, like analog and RF (Radio Frequency) components, passive elements, power transistors, sensors, actuators and even devices which can be considered beyond traditional paradigms as biochips, fall into this new category. Systems included there are not so well-defined as their opportunity is driven by market needs combining to technological feasibility (including cost).

Finally, there is a third coordinate that, although tightly related to the More-than-Moore concept, worth considering as a separate entity. It is the incorporation of heterogeneity into integrated systems. In that sense, there are two already coined names to include the cases under focus nowadays: System-on-Chip (SoC) and System-in-Package (SiP). This is illustrated by Figure 2-c, where both concepts are represented. In fact, SoC is a general name for systems including any class of devices on a common semiconductor substrate. When this is the case, interactions with the external world are only done in the actual periphery of the system, avoiding perturbations due to interconnect with the own system components. Of course, there are other problems caused by the common substrate, and they need to be adequately circumvented. Similarly, SiP corresponds to systems where components can be fabricated in the most convenient technology as they

are finally assembled in a way that reduces the interactions with the external environment.

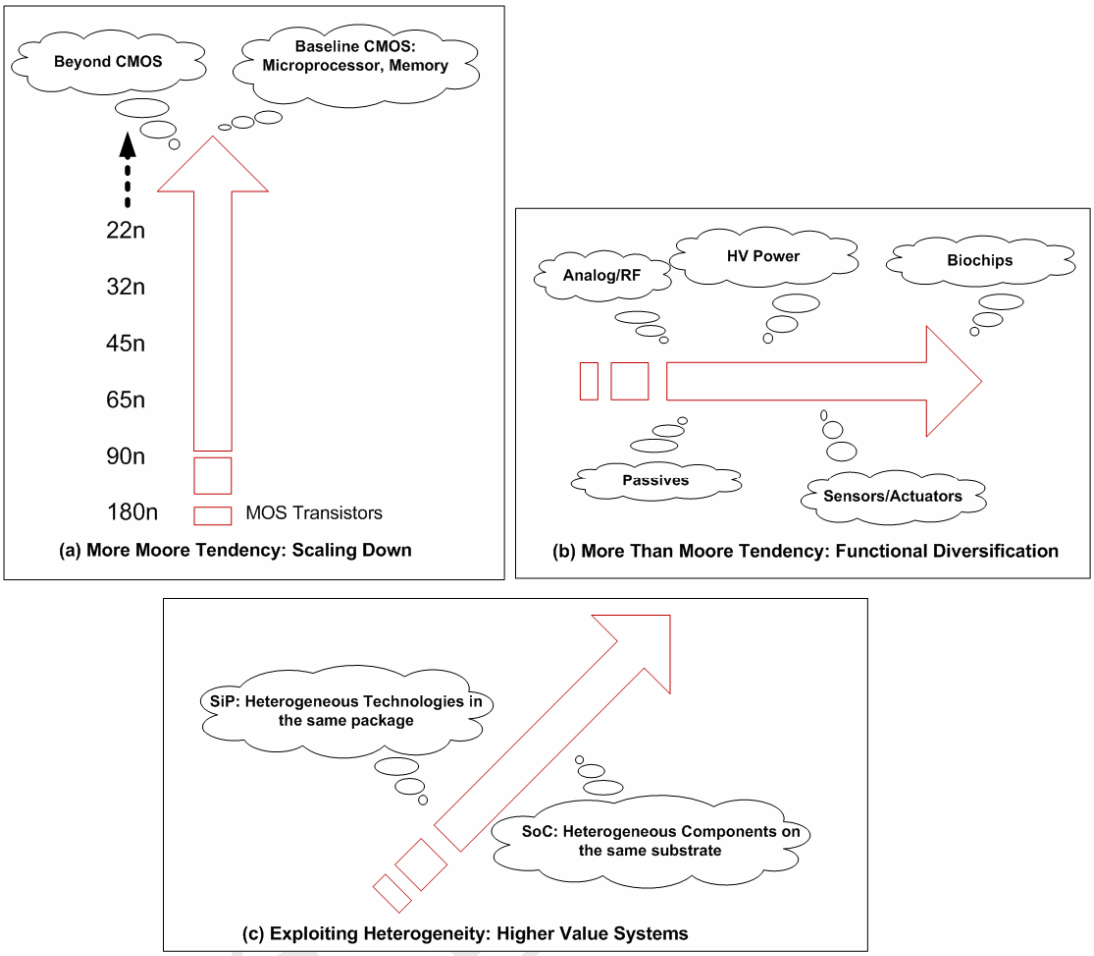

Figure 2. Coordinates defining VLSI evolution

Then, the term VLSI has no longer just a meaning related to the number of transistors but to the complexity a chip may have. Any integrated circuits including either or both a) a huge number of digital devices, b) many digital and non-digital devices (analog, RF, sensors, actuators,…) are considered VLSI as they are hard to design and put on the foreground many usual requirements to be taken into account when these chips have to be designed, fabricated and tested. Besides that, these systems can be realized or not on the same semiconductor substrate, giving a high flexibility in terms of market acceptance.

In this sense, we can admit as an updated definition of the term the following: VLSI is a term associated with the integration of dense and complex chips forming a system, without a precise quantitative measure of any of these two properties (density and complexity); these systems can be realized on the same semiconductor substrate or combining different ones but connected by semiconducting wires. Then, the three coordinates previously introduced combine into a design space as shown in Figure 3, which is the space in which any modern-days VLSI must exist.

Although the vision given in Figure 2 may induce the idea that we are handling three coordinates we can deal independently with, this is not true. In fact, that Figure is just a conceptual high-level view of the problem. Actually, interactions among the three coordinates are very strong, making difficult even a clear separation. As has been mentioned, a more realistic vision can be obtained from Figure 3, where the VLSI design space is represented as two-dimensional since SoC or SiP are tackled when higher-value systems are the target.

Keeping in mind the wide definition given above and the close relationships involved within Figure 3, it should be clear that there are a number of significant topics having a key influence on the efficiency of modern VLSI circuits. We can summarize the most important ones:

- Advanced MOS Technologies
- Deep Submicron Design and Modeling Issues, including methods to handle process variations through the incorporation of statistical design techniques.
- Logic and High-Level Synthesis
- Digital systems and architectures
- Digital Signal Processing and Image Processing IC Design
- Analog, Mixed-Signal (MS) and Radio Frequency (RF) IC Design
- Testability and Design for Test
- CAD Tools, from specialized design tools to design frames, including design flows.
- Interconnects, 3-D Integration and Physical Design
- Low-Power and Thermal-Aware Design, including power management and methods to reduce dynamic power dissipation in scaled technologies, like dynamic bias or frequency scaling
- Timing and clocking issues: clock generation and distribution, time verification, clock skew, asynchronous techniques.
- SoC Design: non-electrical model, MOS-compatible microsensors…
- New Architectures and Compilers, Reconfigurable Systems
- Prototyping, Validation, Verification, Modeling and Simulation
- Embedded Systems Design, Hardware-Software Co-design and Real-Time Systems

When globally considering its evolution along years, we can state that, since the times when the VLSI term was introduced, there has been a lot of changes conditioning the important issues having an influence on this concept. First of all, the evolution of technology, which has shrunk down below barriers not even envisioned in those first times. This evolution translated into a higher number of devices per chip, in accordance to Moore's Law. However, this has also influenced other design constraints. One of them is power density. As devices are going smaller, power density has increased several orders of magnitude, requiring new methods to dissipate the heat. Related to dimensions as well, there is an ever increasing problem: reliability is severely affected due to dimension reduction combined with power dissipation. The fact is a decreasing on reliability. Another impact of technology evolution is the need to cope with parameters affected by larger random variations, thus forcing the designer to use more and more statistical design tools and incorporating more complex models for transistors

and connections. Since most circuit properties are correlated, techniques at different abstraction level must be considered. For instance, increasing speed requires increasing bias voltages, which also increases power dissipation. A popular technique at system-level is to benefit of the maximum speed only where and when is really needed. To do that, several bias voltages are used instead of a single value. Then, higher bias will be used for high-speed, high-power parts and lower supplies for those parts where energy has to be saved.

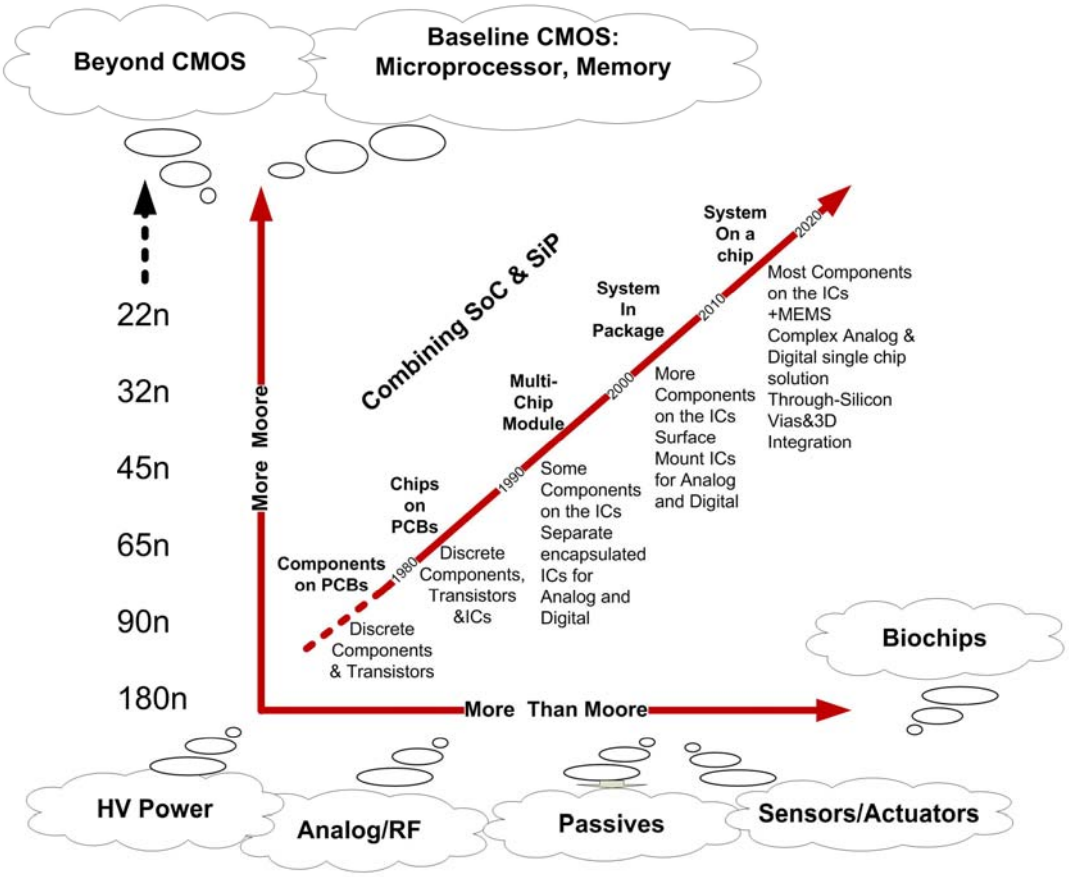

Figure 3. VLSI Design Space

Coexistence of analog and digital components on the same semiconductor substrate also poses new problems. A common substrate facilitates undesired interactions between both kinds of components. Digital noise is spread all over the chip and may cause troubles during the operation of analog circuitry [3]. Methods to reduce substrate coupling or to isolate the analog parts are essential to the operation of complex VLSI nowadays.

Interconnection is another important issue. The number of external pins is very limited for modern VLSI chips, what means a reduced mechanism for interaction with the external world. The consequences are twofold. First, most pins are reserved for biasing, grounding, and continuous time signals, being quite a few the number of digital access ports. A second consequence, related to the previous one, is that testing is becoming cumbersome. Testing digital devices is more and more difficult due to the restricted pin

number [4]. Moreover, a real-life testing implies the simultaneous at-speed testing of analog and digital subsystems. This is particularly difficult due to the ad-hoc nature of analog test as well as to the lack of enough access terminals to readout the test signals outputs. Specific tests for such complex systems are under study [5]. For digital circuitry, there exist general test techniques since long ago, which can be considered adequate. However, for such complex digital systems, there is not always possible to find efficient solutions. Today digital fault models, for advanced technologies, are complex and not so well-established as they used to be in the past. Traditional fault models like stuck-at models are not reflecting the kind of faults one may find in modern MOS technologies. Even more, failure mechanisms as those affecting microsensors (or nanosensors) are far from being satisfactorily modeled at an electrical level.

New interconnects are then under development, like 3-D integration, which addresses the construction of SiP as an alternative to complex SoC. This idea is based on mounting together (one on top of another) two or even more chips, connecting them through silicon vias. The gain is a higher density as well as the advantages of using different MOS technologies for every chip. However, power dissipation may be still a problem as well as semiconductor vias are not yet mature.

Timing is also an issue. For large chips, efficient clock distribution is quite a formidable task [6]. For totally-synchronous designs there are problems related to clock skew, clock power consumption, clock distribution along the chip, fan-out, etc. And this is even more complex when there are mixed-signal components, which usually also require a clock. Asynchronous or partially-synchronous techniques are beginning to be popular, although their disadvantages are not always compensated by their advantages. Besides the fact that asynchronism may avoid problems related to the clocking itself, this also reduces power dissipation, since the chip activity is restricted to the processing events. In other words, instead of a periodic activity controlled by the clock, circuit parts which are not operative can be asleep. Even mixed-signal circuitry (basically, data converters) are now targeting the use of a non-synchronous paradigm.

As far as sensors and actuators are incorporating to VLSI, there are other difficulties related to technology and its modeling. Sensors and actuators may require non-electrical models which have to be compatible with the regular design flow, based on electrical simulators. Both, the incorporation of these extended models and the design flow extensions or modifications, must be targeted in modern days VLSI research.

Talking about design flows, the incorporation of non-digital devices forces to much more complex flows, where compatibility between components is essential. In addition, verification issues are more and more needed since guaranteeing a first-silicon working is not an easy task. Design flows and their associated tasks are supported by CAD (Computer Aided Design) tools, which are also becoming more complex and since long ago are integrated in the so-called design frameworks and platforms. The number and diversity of tools to be used are dependent on the particular chip to be realized.

Topics related to the digital world can be considered mature enough in the frame of complex VLSI. Nevertheless, all these topics need some revisiting since a) complexity increasing has an impact on them, and b) they need to coexist with More-than-Moore

devices with which digital circuitry has to cooperate within the chip. Architectural issues need also to be adapted to manage with efficiency non-digital subsystems as well.

Most topics listed above can be further grouped into categories related to the abstraction level from which a VLSI circuit is contemplated. In this sense, we can consider three basic ones, starting from the more abstract to the more physical:

- Architectural
- Circuit Design
- Technology-related

And one additional category which refers to aspects linked to the above-listed abstraction levels, and what we may call

- Complementary

In what follows, every category will be reviewed with the aim of offering the flavor of its role within VLSI system creation. Although some of these categories may have connections to more than one abstraction level, for the sake of simplicity, we have decided including in every category just those topics which are relevant for this.

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Bibliography

[1] Y. Taur, T. H. Ning. (2009). *"Fundamentals of Modern VLSI Devices"*. Cambridge University Press. [A widely adopted standard textbook in many major US universities and worldwide to learn the basic properties and designs of modern VLSI devices, as well as the factors affecting performance]

[2] G. E. Moore. (1979). *"Are We Really Ready For VLSI?"*. IEEE International Solid-State Circuits Conference. 54-55. [A review and some observations on the trends of microelectronic industry]

[3] F. Moll, M. Roca. (2004). *"Interconnection noise in VLSI circuits"*. Kluwer Academic Pub. [It is intended for providing the notions required for solving the interconnection noise problem in VLSI Circuits]

[4] M. Burns, G. W. Roberts. (2001). *"An Introduction to Mixed-Signal IC Test and Measurement"*. Oxford University Press Inc., New York. [It is a textbook for advanced undergraduate and graduate-level students as well as engineering professionals encompassing the testing of both analog and mixed-signal circuits including many borderline examples].

[5] J.L.Huertas (Editor) (2004). *"Test and Design-for-Testability in Mixed-Signal Integrated Circuits"*. Kluwer Academic Publishers. [It deals with test and design for test of analog and mixed-signal integrated circuits, especially in System-on-Chip (SoC), where different technologies are introduced (analog, digital, sensor, RF, …)]

[6] T. Xanthopoulos *(ed.)* (2009) *"Clocking in Modern VLSI Systems"*. Springer. [It covers a wide range of subjects related to microprocessor clocking including distribution, flop design, inductive techniques,

phase noise and jitter, delay lock techniques, resiliency and other techniques to address process variation and physical design aspects]

[7] D. Gajski, N. Dutt, A. Wu, S. Lin. (1992).*"High-Level Synthesis. Introduction to Chip and System Design"*. Kluwer Academic Pub.[It is a textbook on high-level synthesis and includes the basic concepts, the main algorithms used in high-level synthesis and a discussion of the requirements and essential issues for high-level synthesis systems and environments]

[8] D. Gajski, F. Vahid, S. Narayan, J. Gong. (1994). *"Specification and Design of Embedded Systems"*. Prentice-Hall, [A book on embedded systems which offers a unified approach to hardware and software specification and design issues - and outlines a specify-explore-refine paradigm that is used in industry]

[9] J. Rozenblit, K. Buchenrieder (1994). *"Codesign Computer-Aided Software/Hardware Engineering"*, IEEE Press. [A collection of 21 invited chapters by leading researchers and practitioners. It covers all the latest research developments as well as practical applications on software/hardware co-design, showing how to achieve optimal functionality and to reduce system development time through the concurrent refinement of heterogeneous systems]

[10] S.O. Memik, R. Kastner, E. Bozorgzadeh, M. Sarrafzadeh. (2001). *"A Scheduling Algorithm for Optimization and Early Planning in High-level Synthesis"*, ACM Transactions on Design Automation of Electronic Systems. [http://www.ics.uci.edu/~eli/publications/journal/sched-todaes.pdf]

[11] Tseng, C.J., Siewiorek, D.P. (1983). Facet: A Procedure for the Automated Synthesis of Digital Systems. Proceeding of the 20th ACM/IEEE Design Automated Conference, 490–496. [This describes an automatic data path synthesis program which partially explores the design space]

[12] P. Michel, U. Lauther, P.Duzy. (1992). *"The Synthesis Approach to Digital System Design"*. Kluwer Academic Publishers, Norwell, MA, USA, 415 pp. [A reference and a textbook that provides a broad comprehensive presentation of state-of-the-art techniques and algorithms used in high-level design description, synthesis and verification]

[13] M.A. Bayoumi (1994). *"VLSI Design Methodology for Digital Signal Processing Architectures"*, Kluwer Academic Publishers, Norwell, MA, USA, 420 pp.[This is centered around a number of emerging issues in this area, including system integration, optimization, algorithm transformation, impact of applications, memory management and algorithm prototyping]

[14] M. Ciletti. (1999). *"Modeling, Synthesis, and Prototyping with the Verilog HDL"*, Prentice-Hall, Upper Saddle River, New Jersey, USA, 724 pp.[This aims to introduce new users to the language of Verilog with details on how-to-write hardware descriptions in Verilog in a style that can be synthesized by readily available synthesis tools]

[15] (1999) *"The Digital Signal Processing Handbook"*, V. K. Madisetti and D. B. Williams, CRC Press LLC, 1760 pp.[This volume provides an accessible reference, offering theoretical and practical information to the audience of Digital Signal Processing users]

[16] L. Tan (2008). *"Digital Signal Processing: Fundamentals and Applications"*. Academic Press, 840 pp.[This textbook presents digital signal processing (DSP) principles, applications, and hardware implementation issues, emphasizing achievable results and conclusions through the presentation of numerous worked examples, while reducing the use of mathematics for an easier grasp of the concepts]

[17] E. Lai (2004). *"Practical Digital Signal Processing for Engineers and Technicians"*, Newnes, 304 pp.[This introduces the general area of Digital Signal Processing from a practical point of view with a minimum of mathematics]

[18] G. Proakis, D. K. Manolakis (2006). *"Digital Signal Processing: Principles, Algorithms, and Applications"*. Prentice-Hall. 1004 pp. [This book presents the fundamentals of discrete-time signals, systems, and modern digital processing and applications for students in electrical engineering, computer engineering, and computer science]

[19] V. Oppenheim, R. W. Schafer, J. R. Buck (1999). *"Discrete-time Signal Processing"*. Prentice-Hall, 870 pp. [A text on Digital Signal Processing providing thorough treatment of the fundamental theorems and properties of discrete-time linear systems, filtering, sampling, and discrete-time Fourier Analysis]

[20] J. Rabaey, A. Chandrakasan, B. Nikolic (2002).*"Digital Integrated Circuits: A Design Perspective"*, Prentice-Hall, . [Progressive in content and form, this practical text successfully bridges the gap between the circuit and the system perspectives of digital integrated circuit design]

[21] N. Weste, D. Harris (2005).*"CMOS VLSI Design"* Addison-Wesley, 800 pp. [This book details modern techniques for the design of complex and high performance CMOS Systems-on-Chip]

[22] B. Razavi (2000). *"Design of Analog CMOS Integrated Circuits"*, McGraw-Hill, 684 pp. [This text covers the analysis and design of CMOS integrated circuits that practicing engineers need to master to succeed]

[23] K. Roy, S. Prasad (1999) *"Low power CMOS VLSI circuit design"* Wiley, 376 pp. [A comprehensive look at the rapidly growing field of low-power VLSI design]

[24] W. Wolf (2002). *"Modern VLSI Design: Systems on Silicon"*, 3rd. ed. Prentice-Hall, 592 pp. [The start-to-finish, state-of-the-art guide to VLSI design]

[25] B.Young (2000) *"Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*". Prentice Hall, 560 pp. [This state-of-the-art book provides students with techniques for predicting and achieving target performance levels]

[26] M.J. Ma et al. :*"Suppression of boron penetration in P+ polysilicon gate p-MOSFETs using low temperature gate-oxide N2 O anneal"*.IEEE Electron Device Letters, Vol 15, nº 3, pp 109-111, March 1994. [Annealing effects in the behaviour of thin oxides for MOSFET gates]

[27] Kai Chen, Chenming Hu: *"Performance and V_{dd} scaling in deep submicrometer CMOS"*. Journal of Solid-State Circuits, 33, October 1998, 1586-1589. [CMOS design guidelines and model equations for deep submicronic drain saturation current]

[28] Y.-K- Chain et al.: *"Ultra thin – body SOI MOSFET for deep-sub-tenth micron era"*. IEEE Electron Device Lett., Vol. 21, p 254, 2000. [UTB structure shows elimination of leakage paths in deep-sub-tenth micron CMOS technology]

[29] J.P. Colinge: *"Silicon-on-insulator technology: Materials to VLSI"*. Kluwer Academic Publisher, 2004. [A full review of SOI technologies for microelectronics]

[30] T. Ghani et al.: IEDM 2003, p. 978. [A 90 nm. high volume manufacturing logic technology featuring novel 45 nm. gate lenght strained silicon CMOS transistors]

[31] Jyh- Chyurm Guo: *"Halo and LDD engineering for multiple Vth high performance analog CMOS devices"*. IEEE Trans. on Semiconductor Manufacturing, 20, 3, 2007, pp 313-322. [Multiple threshold voltages CMOS devices fabricated in a 130 nm. technology, using Halo and LDD combined with a unique dual gate oxide module, for aggressive gate oxide thickness scaling]

[32] Chang-Hoon, P.R. Chidambaram, Rajesh Khamankar, Charles F. Machala, Zhiping Yu, Robert W. Dutton: "Dopant profile and gate geometric effects on polysilicon gate depletion in scaled MOS*". IEEE Trans. On ED*, 49, nº 7, July 2002, pp 1227-1231. [Vertical and lateral polysilicon gate simulation of dopant profiles and potential drop as the MOS capacitance geometry is scaled down]

[33] Igor Polishchuk et al.: "Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion". *IEEE Electron Device Letters*, Vol. 23, nº 4, Abril 2002, p. 200. [Threshold voltage adjustment in P and N type MOSFETs by means of Ni contents of Ti based metal gate structures]

[34] Y.-C. Yeo et al.: "Effects of high-K gate Dielectric Material on metal and silicon gate work functions". *IEEE Elec.Dev*. Lett., Vol. 23, nº 6, 2002, pp 342-344. [In this paper the dependence of metal and polysilicon gate work-functions on the underlying gate dielectric in advanced MOS gate stacks, is explored]

[35] C.M. Osburn et al.: *"Ultra shallowjunctions formation using very low energy B and BF2 sources"*.11th International Conference on Ion Implantation Technology, Aug. 2002, pp. 607-610. [Fabrication of very shallow PN junctions using B and BF_2 ion implantation]

[36] J. Gautier: *"Physics and operation of silicon devices in integrated circuits"*. ISTE, Wiley, 2009. [MOS and bipolar transistor physical main issues surrounding the current state-of-the-art in microelectronic technology]

[37] S.B. Samavedam et al.: "Elevated source drain devices using silicon selective epitaxial growth". *J. Vac. Sci. Technol*. B, Vol. 18, pp. 1244-1250, 2000. [Fabrication of self-aligned ESD structures in conventional CMOS processes for reducing parasitic series resistance, achieving also shallow contacting junctions.]

[38] C. Wang et al.: "Sub-40nm Pt Si Schottky source/drain metal-oxide-semiconductor field-effect transistors". *Appl. Phys. Lett*, Vol. 74, pp. 1174-1176, 1997. [Fabrication of Schottky type S/D junction MOSFET for sub-40 nm.technolgy, showing a reduction of delay times]

[39] B. El – Kareh: "*Fundamentals of semiconductor processing technology*". Kluwer Academic Publishers, 1995. [A review of the main semiconductor processes for being used in microelectronic technologies]

[40] M. Levenson et al.: "Improving resolution in photolithography with a phase-shifting mask ". *IEEE Trans. Electron Dev*., ED-29, pp. 1828-1836 (1982). [Phase-shifting mask process description, showing results for a 1000 lines /mm resolution.]

[41] Hammah et al.: "*Integrated circuits 3D silicon integration*". ICONS' 09, March 2009, 204-209. [A review on driving forces and trends for shifting from planar microelectronics to 3D technologies]

[42] Y.K. Choi et al.: "Nanoscale CMOS spacer FinFET for the Terabit Era". *IEEE Elec. Dev. Lett*., Vol. 23, 2002, pp. 25-27. [Description of a spacer lithography process technology, using a sacrificial layer and a CVD grown spacer layer, for a double-gate FinFET structure fabrication]

[43] K.K. Likarev:"Single electron devices and their application". *Proc. IEEE*, 87, April 1999, pp. 606-632. [Review of the basic physics of single electron devices as well as their current and prospective applications]

[44] Tans SJ, Verschueren ARM, Dekker: "Room-temperature transistor based on a single carbon nanotube". *Nature*, Volume 393, Page 49-52, 1998.[Fabrication of a new one-molecule electronic three-terminal switching device, based on a single wall carbon nanotube]

[45] S. Thomson et al.: "130nm logic technology featuring 60nm transistors, low-K dielectrics, and Cu interconnects". *Intel Technology Journal*, Vol. 6, nº 2, pp. 5-13, 2002. [Description of Intel's 130 nm. CMOS logic technology, used to make high performance microprocessors > 3 GHz.]

[46]http://www.electroiq.com/index/display/packaging-article-display/359086/articles/advanced-packaging/packaging0/integration/tsv/2009/04/3d-ic-technology-interconnect-for-the-21st-century.html. [Description of a 3D IC technology, where thinned planar circuits are stacked and interconnected using through silicon vias (TSVs)]

[47] M.L.Bushnell, V.D.Agrawal (2004) "*Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits*", Kluwer Academic Publishers. [Today's electronic design and test engineers deal with several types of subsystems, namely, digital, memory, and mixed-signal, each requiring different test and design for testability methods. This book provides a careful selection of essential topics on all three types of circuits]

[48] D. D. Gajski,S. Abdi,A. Gerstlauer,G. Schirner (2009). "*Embedded System Design: Modeling, Synthesis and Verification*", Springer. [This book presents information on how to design a future multiprocessor system consisting of several processors and other components]

[49] P. van der Wolf (1994). "CAD Frameworks: Principles and Architecture", Kluwer Academic Publishers, 236 pp. [This book describes the design and construction of CAD frameworks]

[50] Course:"*Trends in VLSI Design: Methodologies and CAD tools*". Presenter Raj Singh. IC Design Group, CEERI, Pilani-333031.

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