

ANALOG CIRCUITS

Paul G.A. Jaspers

Catholic University of Louvain. Louvain-la-Neuve, Belgium.

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Summary

A MOS inverter is considered in order to illustrate the design of a simple analog circuit. Transistor models are reviewed and concepts such as activity, power and voltage gain discussed. To realize fast, reliable and accurate networks, analog designers take advantage of matching, parallelism, feedback etc... The Miller operational amplifier paves the way towards precision analog circuits. In an increasingly numerical world, A to D and D to A converters are the ultimate link between analog environment and digital systems.

1. Analog versus Digital

While the word ‘Digital’ refers to icons such as mobile telephony, computers, etc... ‘Analog’ doesn’t wake up identical images. Consider for instance digital versus analog cameras. Both make use of the same imagers. In the digital camera the analog video signal is compared against a large number of discrete levels and the result coded

accordingly. In the analog camera the output signal consists of voltages or currents. The first outputs bits, the second analog data. The fact that the performances of digital cameras outdo those of analog cameras does not mean however that 'analog' is synonymous to obsolescence. A more cautious answer is anticipated owing to our environment, which is analog in essence. Assessing light, temperature, forces, velocity, etc. requires sensors, which convert mostly analog physical data into voltages or currents. In the imager for instance, light discharges elementary photodiodes, called 'pixels'. After a short time interval, called the light integration time, the amount of charge needed in order to restore initial conditions is measured. Now that the image is turned into discrete charge packets, these are converted into voltages, still analog data thus. The conversion to digital data takes place only after this.

Filters illustrate another aspect of the comparison analog versus digital. Filtering can be done either in the frequency domain or in the time domain. Analog filters operate in the frequency domain, digital filters in the time domain. A long time ago, filters were exclusively analog devices. They were made of passive elements, capacitors and inductors. An interesting alternative came about with the introduction of Operational Amplifiers since these take advantage of resistors, capacitors and don't need inductors. Digital implementations were totally ignored until the advent VLSI circuits, which paved the way towards the possibility to implement large digital systems.

Digital filters are actually hardware counterparts of mathematical algorithms implementing the behavior of analog filters. Since the length of the data words determines the accuracy, digital filters ignore mismatch, aging etc, which affect currently analog filters. Produced in large quantities digital filters are more economical than analog moreover for they don't require external precision elements. Why analog filters then?-because at high frequencies analog filters are much faster. To give an example, consider the front end of a mobile telephone. Selecting a communication channel in the digital domain is not feasible for the frequencies of the signal that must be discriminated are of the order of GHz. That does not mean that mobile phones do not take advantage of digital signal processing as well. Once the desired channel is isolated and the frequency lowered, digital signal processing starts taking place. Both digital and analog cooperate thus. Another interesting aspect is power consumption. Analog filters consisting of reactive elements don't take up power.

It is worth mentioning that a number of circuits assimilated currently to digital blocks are in fact true analog circuits. A striking example is given by dynamic memories. The data stored in the memory consist of charges stored across large arrays of very small capacitors. To read out the content of the memory, every capacitor can be connected to a read out line by means of a MOS transistor, which plays the role of a switch. A row and a column address derived from a decoder control the switch.

Because the capacitance of the read-out line is much larger than that of the memory cell, the voltage step across the line caused by the signal stored in the cell is divided by a factor that can be larger than 10. The read out signal is very little thus compared to the voltage difference that is expected between a logical one and a zero. The signal needs to be amplified consequently in order to restore the data. This requires an amplifier that separates the signal from unavoidable switching noise. The MOS transistor connecting

the cell to the read-out line is likely to introduce unwanted charge indeed from the MOS switch itself. Though small, this charge can corrupt the output data. To avoid false readings, read-out circuits do not evaluate the magnitude of the voltage step on the read out line but the difference with respect to the voltage across a dummy line terminated by a similar cell storing either a fixed zero or a one. Since the dummy line is supposed to have the same parasitic capacitance as the read out line, switching noise boils down to a common mode signal that is discriminated by means of a differential amplifier.

At the output of the amplifier, the signal is large enough to be assimilated to a zero or a one and ready to be stored in a bistable circuit. Though the output of the memory is a logical signal, what happens inside is far from Boolean algebra. The same holds true for static memories. Though static memories make use of arrays of flip-flops and the data true ones and zeros, writing and reading requires input/output lines and switches. Once again, this introduces parasitic capacitances larger than the node capacitances of each individual cell. Appropriate analog circuitry is needed in order to prevent false readings.

Telecommunication systems like memories show clearly that when it comes to high performance circuits, the boundary between analog and digital circuits is not so clear anymore. Advanced digital circuits even cannot be reduced to zeros and ones only. Beyond 10 GHz, transistors cannot be assimilated to static devices anymore and the interconnections require taking into consideration the time signals need to travel from one gate to another.

The impact of capacitive coupling cannot be overlooked either. The substrate cannot be considered as a reference plane for the voltage drops caused by ground currents affect the back gate of MOS transistors. It is clear that a mix of design skills involving modeling, simulation, analog circuitry, signal processing and even solid state physics is required to deal efficiently with these effects.

To illustrate the nuts and bolts of analog design, we consider in the next section a simple example: a single transistor amplifier, which can be viewed as a logical inverter too. The analog designer is concerned by the linearity of the amplifier, its gain-bandwidth product, linearity and noise. The digital designer looks for the shortest switching time from a 'one' to a 'zero' or vice versa.

What the 'zeros' and 'ones' represent is not critical for the digital designer provided an unambiguous distinction can be made between states. It doesn't matter whether a 'zero' or a 'one' correspond respectively to 0 Volt and to the supply voltage or whether the signals move away from these limits. Gain is not an issue either.

Most logical circuits display gains lower than 10. A gain slightly larger than 2 is sufficient to implement a regenerative circuit like a flip-flop. What the digital designer is much more concerned with is the ever-shorter gate lengths offered by the technology. These allow to design faster circuits that consume less energy per cycle, a crucial item when dealing with billion transistors chips.

The items considered in this chapter are intended to illustrate typical analog circuit design techniques and the systematic recourse to feedback, matching, layout, statistical

averaging, etc in order to achieve high performances, fast, reliable and accurate circuits. We start with the basic bloc common to digital and analog circuits: the inverter.

2. The Basic Inverter

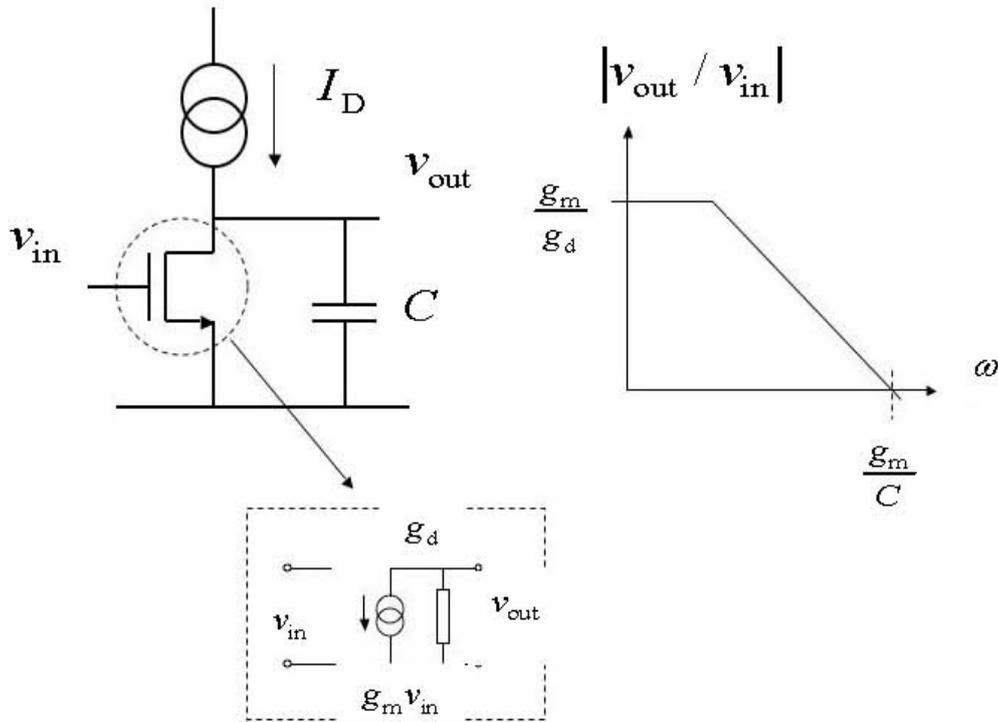


Figure 1. The MOS inverter

Inverters are the backbone of electronic circuits whichever function, logic or analog. The elementary inverter boils down to a common emitter or common source transistor (depending on the type of transistor) fed by a current source. The left part of Figure 1 shows a MOS inverter loaded by a capacitance.

2.1. Analysis

To evaluate the performances of the inverter, the transistor is replaced generally by an 'equivalent circuit'. Many equivalent circuits have been proposed over time, some very simple other more accurate but also more complex. The one shown in the lower part of fig 1 is a simple linear circuit that mimics the behavior of the MOS transistor as long as the input/output voltage excursions do not depart substantially from steady state conditions. These are set by means of bias circuitry not shown in the figure. We represent the departures from the DC gate-to-source voltage V_{in} , drain-to-source voltage V_{out} and drain current I_D respectively by means of lower case symbols, v_{in} , v_{out} and i_D .

The gate voltage controls the drain current i_D by means of the dependent small signal current source $g_m v_{in}$. At low frequencies the drain current i_D flows preferably through the conductance. At high frequencies, the capacitor takes over. The corresponding output/input voltage ratios are:

$$1) \text{ At low frequencies: } v_{\text{out}}/v_{\text{in}} = -g_m/g_d \quad (1)$$

$$2) \text{ At high frequencies: } v_{\text{out}}/v_{\text{in}} = -j\omega/(g_m/C) \quad (2)$$

These expressions lead to the frequency response displayed in the right part of Figure 1. At low frequencies, the inverter ‘amplifies’ the input signal. At high frequencies, the capacitance shorts progressively the conductance lessening gain. The frequency performances of the amplifier are assessed generally by the ‘angular transition frequency’ ω_T , also called the ‘gain-bandwidth product’, which boils down to the ratio of the transconductance g_m over the load capacitance C .

2.2. Synthesis

Analog designers must determine the gate length L , the width W and the DC current I_D of MOS transistors so as to meet predefined specifications, e.g. a desired gain-bandwidth product. There is no unique solution so that one can take advantage of any freedom degree left open to take into consideration additional objectives such as a large gain, minimal power consumption etc...

How to choose optimal dimensions and the drain current I_D so as to make g_m equal to $\omega_T \cdot C$. One possibility is to estimate the gate length and width making use of a transistor model and to check the results by taking advantage of a simulation tools like Spice, BSIM and PSP. These are accurate industrial standards exploiting a large number of proprietary data that are determined generally by the silicon foundries where chips will be manufactured. They are suited for verification purposes but not so much for sizing. Evaluating sizes and currents requires expressions that are simple enough to offer the possibility to assess design challenges. This is not possible with simulators unless indirectly. The question is to have at one’s disposal a *large signal equivalent circuit* that is simple enough. Simple models like those described below are appropriate for they give birth to simple expressions linking sizes and currents to the objective(s) to attain. Unfortunately, the approximations affect also the precision of sizing, making repeated simulations unavoidable.

2.2.1. The Quadratic Model of the MOS Transistor

A simple large signal representation of the saturated MOS transistor is given by the well-known quadratic expression of the drain current:

$$I_D = \mu C'_{\text{ox}} \frac{W}{L} \frac{(V_{\text{in}} - V_T)^2}{2n} \quad (3)$$

where μ represents the mobility, C'_{ox} the gate oxide capacitance per unit area, W and L respectively the width and length of the channel, V_T the threshold voltage and n a factor

slightly larger than one that takes care of the so-called ‘body effect’. Evaluating of the transconductance g_m is straightforward:

$$g_m = \sqrt{\frac{2 \mu C'_{\text{ox}} \frac{W}{L} I_D}{n}} \quad (4)$$

Many W/L ratios and drain currents I_D are likely to meet the specified gain-bandwidth product. Small drain currents are desirable for they offer the benefit to increase gain while lessening the power consumption, at the expense however of large gate widths! This is not a hypothetical assumption for the availability of ever-smaller gate lengths leads to the possibility to augment the W/L ratios without increasing substantially the drain junction parasitic capacitance.

The evaluation of the drain current however implies to revise equation 4. The current of MOS transistors is a combination of drift and diffusion currents indeed. The first is controlled by the electrical field along the channel, the second by the charge density. Drift current (also called conduction current) is dominant as the gate voltage exceeds the threshold voltage V_T by at least 0.2 V. The transistor is then in strong inversion. Below this limit, the diffusion current takes over progressively. The transistor enters moderate and weak inversion. In weak inversion, the drain current increases exponentially with the gate voltage. In moderate inversion the increase is neither exponential nor quadratic. The point is that an increasing number of analog MOS circuits operate nowadays in moderate inversion and the quadratic model does not fit in. A possible contender is the model hereafter.

2.2.2. The E.K.V. Model

The E.K.V. model is a large signal model that provides a fairly good representation of I_D from strong to weak inversion. It is an approximation of the Charge Sheet Model, which bridges circuit design and solid-state physics but, unfortunately, is too complicated to lend itself to sizing. The E.K.V. model in contrast is analytically manageable. According to the model, the drain current of saturated MOS transistors is given by:

$$I_D = I_S (q_F^2 + q_F) \quad (5)$$

where I_S is called the ‘specific drain current’ and q_F the ‘normalized forward charge density’. The specific drain current I_S corresponds more or less to the drain current in the middle of the moderate inversion region:

$$I_S = 2nU_T^2 \mu C'_{\text{ox}} \frac{W}{L} \quad (6)$$

When W/L is made equal to one, the specific current boils down to a technological parameter called the ‘unary specific current’ I_{Su} .

The parameter q_F is a dimensionless quantity that is proportional to the charge density at the source of the MOS transistor. It is larger than 10 in strong inversion and smaller than 0.1 in weak inversion. It is the key parameter that controls not only the modes of operation, but also the ‘pinch-off’ voltage V_P according to the expressions below (where U_T is the so-called thermal voltage kT/q equal to 0.026 V at room temperature [$T = 300$ °K], k being the Boltzmann constant and q the electron charge)

$$V_P = U_T [2(q_F - 1) + \log(q_F)] \quad (7)$$

and:

$$V_P = \frac{V_{in} - V_T}{n} \quad (8)$$

An analytical expression of the small signal transconductance can be derived from the E.K.V. model:

$$g_m = I_D \frac{1}{nU_T(1+q_F)} \quad (9)$$

This is a useful expression. Making g_m equal to $\omega_T \cdot C$ paves the way towards the evaluation of drains currents and W/L ratios achieving the prescribed gain-bandwidth product whichever mode of operation. A set of q_F parameters corresponding to the desired mode of operation is chosen first. Drain currents are extracted from the above equation and W/L ratios inferred from:

$$\frac{W}{L} = \frac{I_D}{I_{Su}(q_F^2 + q_F)} \quad (10)$$

An example is shown in Figure 2, which relates to a 0.35 μm gate length inverter loaded by a 1 pF capacitor that achieves a transition frequency of 100 MHz. The plot represents the ensemble of W/L ratios and drain currents meeting the desired gain-bandwidth product. Circles correspond to moderate inversion, q_F being equal to 0.2, 0.5, 1, 2, and 5 from left to right. In strong inversion, W/L varies like the reciprocal of the drain current. In moderate inversion, W/L increases more rapidly while in weak inversion it gets out of control. When the W/L ratio becomes too large moreover, the drain current starts increasing again, owing to the contribution of parasitic drain junction capacitance.

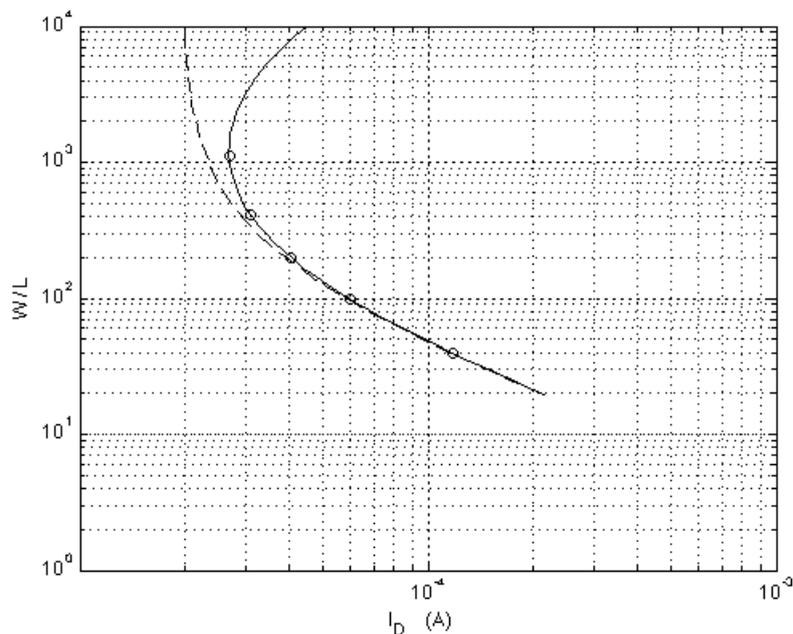


Figure 2. The dotted curve represents W/L ratios versus drain currents of a $0.35 \mu\text{m}$ gate length MOS inverter loaded by 1 pF that achieves a transition frequency of 100 MHz ($n = 1, 2$; $I_{\text{Su}} = 0.1 \mu\text{A}$). The plain curve takes the parasitic drain junction capacitance into account. Circles correspond to q_{F} 's respectively equal to $0.2, 0.5, 1.0, 2.0$ and 5.0 from left to right.

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Biographical Sketch

Paul G.A. Jaspers received the mechanical and electrical engineering degree from the Université Libre de Bruxelles and the doctor degree from the Université Catholique de Louvain (Belgium). He is an Emeritus Professor of the Université Catholique de Louvain where he headed the microelectronics laboratory until 1994. He was also visiting Professor at the University of California Berkeley (1990-91), Stanford University (1967-68), UFRGS (Brasil), UCC (Argentina). He organized several Europractice and Iberchip courses. He was involved in two successive programs for the United Nations Industrial development Organization in India from 1981 until 1994 and lectured in Australia and China. He is still teaching invited courses in France and Italy. His activity is related presently to analog CMOS circuit design with emphasis on A to D and D to A converters and design methodologies. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a former member of the IEEE Solid State Council and the Steering Committee of ESSDERC-ESSCIRC. He is the author of several books (OUP, Springer) and publications in the Journal of Solid State circuits.